
Chrontel CH7039 Multi-Standard Display Interface Converter

FEATURES

- 2 Lane DisplayPort Receiver and Transmitter compliant with DisplayPort specification version 1.2 and Embedded DisplayPort (eDP) Specification version 1.3. Optional HDCP version 1.4, Support VESA and CEA timing standards up to 1920x1200 in 8-bit input with 60Hz refresh rate
- HDMI Receiver and Transmitter compliant with HDMI 1.4 specification and DVI 1.0 specification.
- Support HDMI repeater function.
- Single / Dual channel LVDS 18 / 24 bits receiver and Transmitter supports up to 165 Mpixels/s
- Support 16/18/24 bit parallel video input. Support SDR, DDR, 2X and 3X input timing mode.
- Support BT656 and BT1120 input and output, with embedded or separate sync mode
- Support DP/HDMI 3D input, and output DP/HDMI with repacked 3D content, or output LVDS with R/L View separately. Support LCD panel with resolution up to 1920x1200@60Hz in 2D mode or 1366x768@120Hz in 3D mode
- Three on-chip 9-bit high speed DACs providing flexible output capabilities. Such as single, double or triple CVBS outputs, YPbPr output, RGB output and simultaneous CVBS and S-video outputs
- VGA output is compliant with VESA VSIS v1r2 specification
- Support Component YPbPr output and analog RGB (VGA) monitor up to 1900x 1200 or 1080P
- Advanced pin-multiplexed technology to support multiple input/output display standards
- Support two independent display timing data received simultaneously from two separated input paths
- OSD controller support
- TV / Monitor connection detection capability.
- Support LCD panel protection and power sequencing. PWM is available for controlling LCD backlight brightness. Dynamic backlight dimming to save power consumption Powerful image enhancement engine embedded
- SPDIF audio interface supports either 16-bit or 20-bit stereo data with sampling rate up to 192kHz/2ch.
- Support 2 channel I2S digital audio input and 8(7.1) channel output for up to 24-bit data stream (32kHz/8ch, 44.1kHz/8ch, 48kHz/8ch, 88.2kHz/8ch, 96kHz/8ch, 176.4kHz/8ch and 192kHz/8ch)
- Supports LPCM, One Bit Audio, Dolby Digital, DTS, DSD, HBR digital audio formats

GENERAL DESCRIPTION

Chrontel CH7039 is an innovative display interface product designed for embedded systems, consumer electronics and computing in which conversions among multiple high definition video/audio formats are required. Built in with multiple differential receivers and transmitters, and easy-to-use audio interfaces, the CH7039 can drive LCD panels through either a single or dual channel LVDS/TTL interface or a 1/2 lane DisplayPort interface. It can also simultaneously output to external displays using standards such as HDMI/DVI, YPbPr, VGA, CVBS or S-Video. This device will help manufactures reduce design costs, accelerate time-to-market and expand product features for better user's experience.

The CH7039 has four input and four output ports to supports multiple display standards. Some ports are multiplexed with different signal types to reduce pin count. For example, the 24-bit wide digital port can be programmed to receive LVDS or TTL signals and supports various formats like RGB, BT1120, BT656, etc. while the 8-bit port can accept HDMI or BT656 inputs. The 2 Lane DP / eDP port stands alone because of its high data transfer rate.

Through a 4x2 input switch matrix, the device can be configured to simultaneously accept two separated video formats with independent display timing. The input combination can be mixed among the TTL/BT1120/LVDS, the DP/eDP and the HDMI/BT656 input in either RGB format (RGB-565, RGB-666 or RGB-888 and etc.) or YCrCb format (ITU-R 601/656 and BT1120). A 2x4 output switch matrix can be programmed to drive the various output ports simultaneously with two kinds of independent timing.

The CH7039 supports 3D data structures defined by DP and HDMI standards. The device can translate and repack 3D data when DP signals are converted to HDMI and vice versa. 3D data can also be displayed as R/L frame via its LVDS output.

The CH7039's DisplayPort receiver and transmitter are designed to comply with DisplayPort Specification 1.2 and Embedded DisplayPort (eDP) Specification version 1.3. It provides support for one or two Main Link lanes with data rate running at 1.62Gb/s or 2.7Gb/s. To further optimize the display quality and power dissipation, this device is equipped with seamless display refresh rate switching and progressive to interlace timing switching

- 27MHz is available as crystal or oscillator clock input frequency
- MCU embedded to handle the control logic
- Integrated EDID Buffer
- IO and SPC/SPD supply voltages from 1.8V to 3.3V
- Programmable power management
- Device fully programmable through serial port or can automatically load firmware from On-chip Flash
- RoHS compliant and Halogen free package
- Offered in 176 pin LQFP package and 196 pin BGA package

APPLICATIONS

- Docking Station
- Embedded System
- Notebook / Ultrabook
- Tablet Device
- IPTV Box
- Internet TV / SmartTV
- Video Conversion Cable / Adapter / Matrix
- DVR / Security field
- Stand Show / Medical Inspection Apparatus

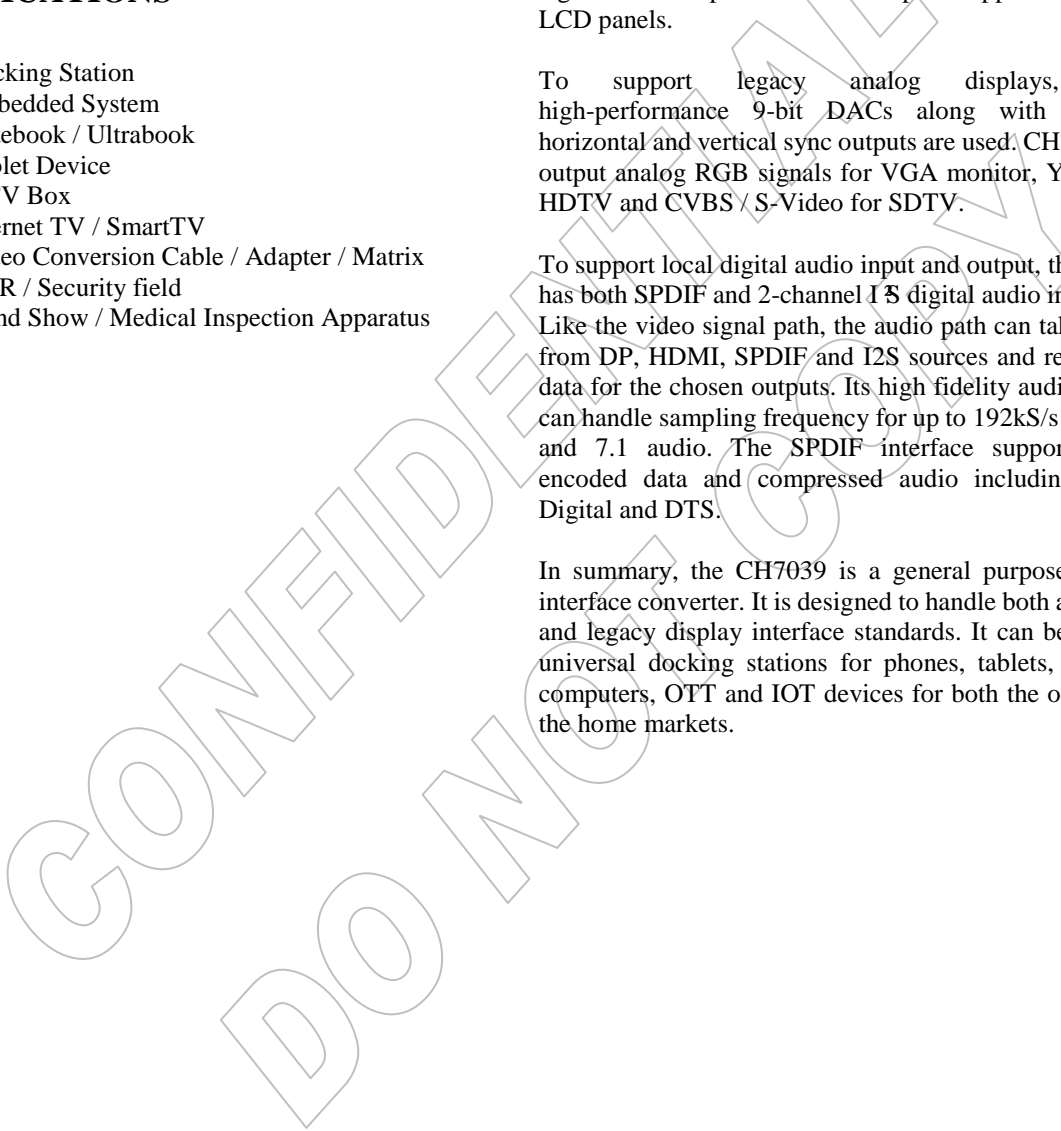
capabilities. The CH7039’s HDMI receiver and transmitter are designed to meet HDMI Specification 1.4 and DVI Specification 1.0. On-chip HDCP cipher engine can be activated to protect the high definition media content.

Dual channel LVDS receiver and transmitter are incorporated into the CH7039. The Panel protection mechanism is also built in to switch off the LCD instantly through device’s automated panel on/off sequences if input data is missing or unstable. The backlight on/off control can be configured through programming internal registers. A built-in PWM generator can be used to adjust display brightness and dimming of the LCD. Dithering algorithm is implemented on chip in support of 18-bits LCD panels.

To support legacy analog displays, three high-performance 9-bit DACs along with separate horizontal and vertical sync outputs are used. CH7039 can output analog RGB signals for VGA monitor, YPrPb for HDTV and CVBS / S-Video for SDTV.

To support local digital audio input and output, the device has both SPDIF and 2-channel I2S digital audio interfaces. Like the video signal path, the audio path can take inputs from DP, HDMI, SPDIF and I2S sources and repack the data for the chosen outputs. Its high fidelity audio engine can handle sampling frequency for up to 192kS/s of stereo and 7.1 audio. The SPDIF interface supports PCM encoded data and compressed audio including Dolby Digital and DTS.

In summary, the CH7039 is a general purpose display interface converter. It is designed to handle both advanced and legacy display interface standards. It can be used in universal docking stations for phones, tablets, personal computers, OTT and IOT devices for both the office and the home markets.



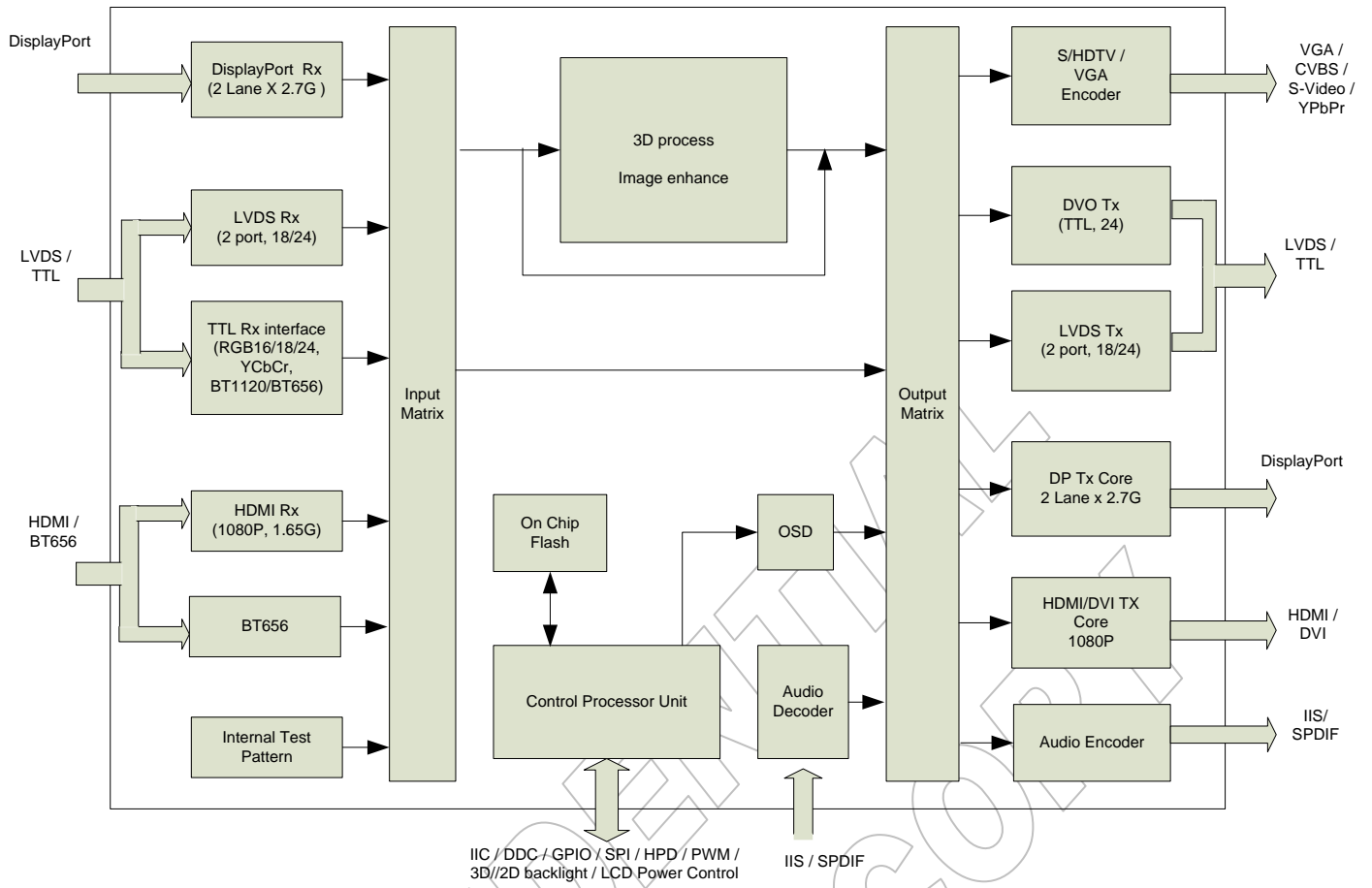


Figure 1: CH7039 Functional Block Diagram

CONFIDENTIAL
DO NOT COPY

1.0 PIN-OUT

1.1 Package Diagram

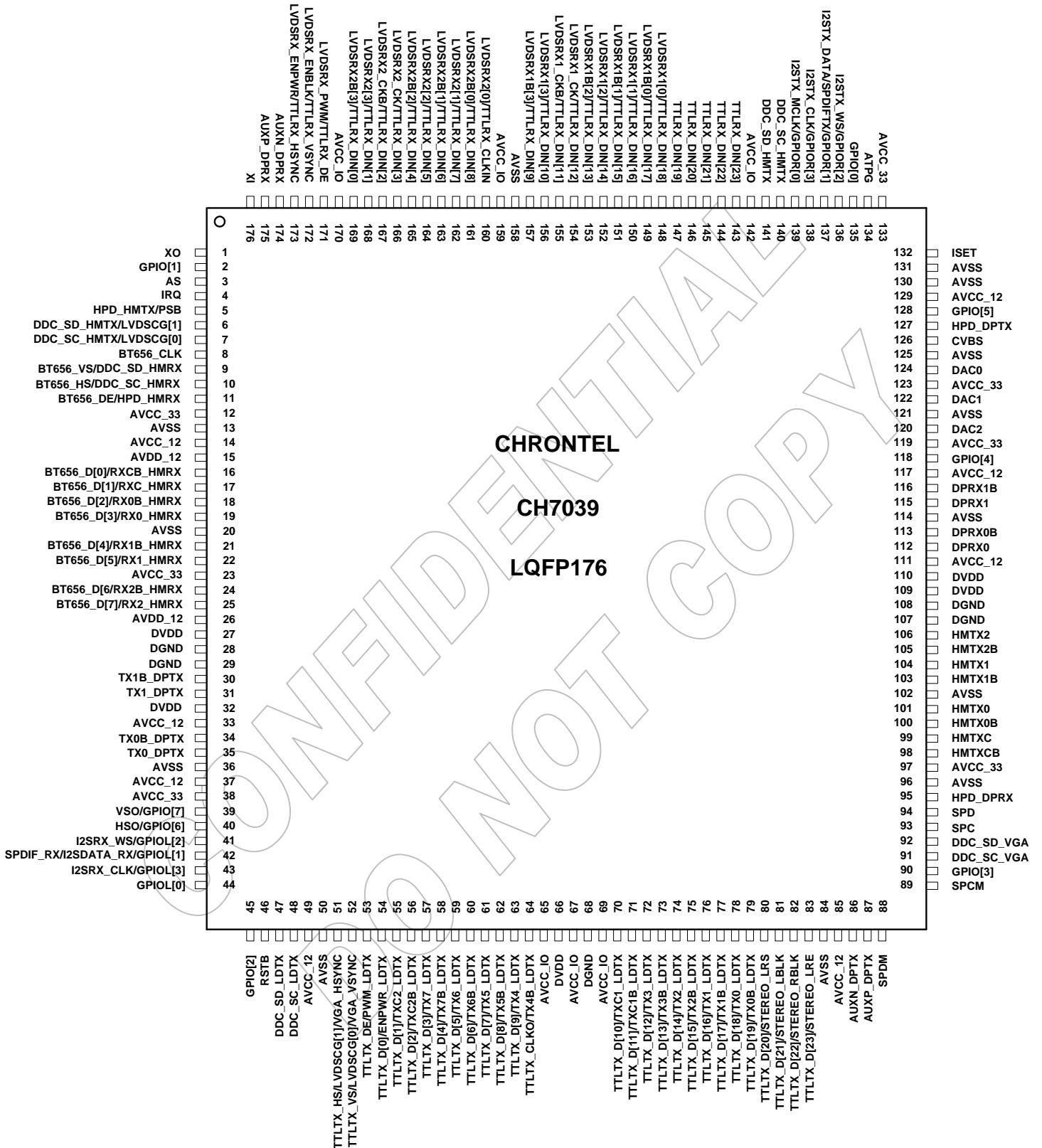


Figure 2: CH7039 176-Pin LQFP Pin Out

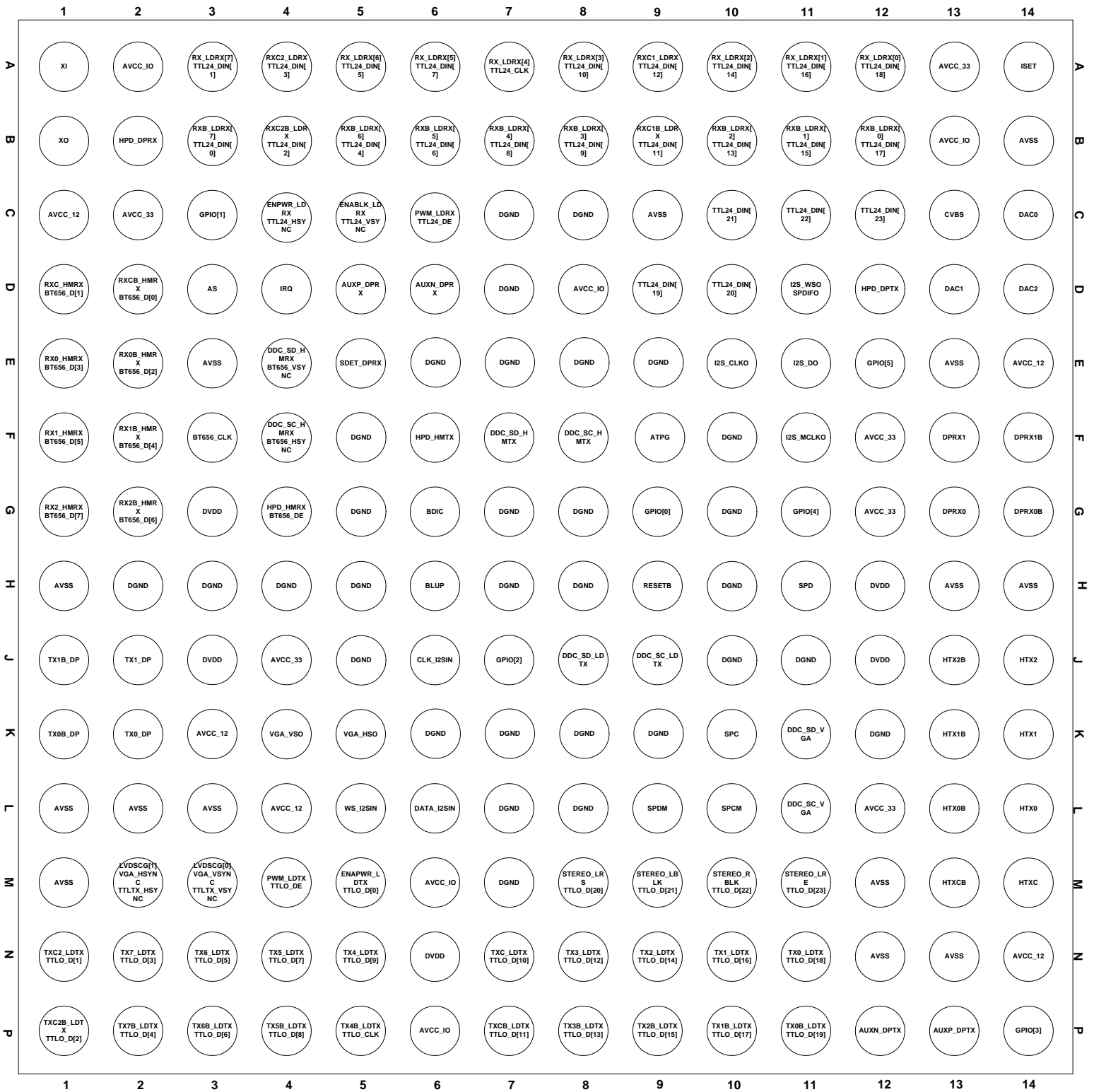


Figure 3: CH7039 196-Pin BGA Pin Out

1.2 Pin Description

Table 1: 176 LQFP Pin Name Descriptions

| Pin # | Type | Symbol | Description |
|---------------------------------------|--------|-------------|--|
| 1 | Out | XO | Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. |
| 2,39,40, 45,90,11 8,128,13 5 | In/Out | GPIO[7:0] | General Purpose Input/Output |
| 3 | In | AS | Address Select |
| 4 | Out | IRQ | Programmed Interrupt Output |
| 5 | In | HPD_HMTX | HDMI Transmitter HPD Input |
| | In/Out | PSB | General Purpose Input/Output |
| 6 | Out | DDC_SD_HMTX | HDMI Transmitter DDC Data Channel This pin functions as the bi-directional data pin of the serial port to HDMI DDC source. This pin will require a pull-up 1.8 kΩ Resistor to the desired voltage level. |
| | In/Out | LVDS CG[1] | General Purpose Input/Output Default definition is LVDS Panel Selection control |
| 7 | In/Out | DDC_SC_HMTX | HDMI Transmitter DDC Clock Channel This pin functions as the clock bus of the serial port to HDMI DDC source. This pin will require a pull-up 1.8 kΩ Resistor to the desired voltage level. |
| | In/Out | LVDS CG[0] | General Purpose Input/Output Default definition is LVDS Panel Selection control |
| 8 | In | BT656_CLK | BT656 Input Clock |
| 9 | In | BT656_VS | BT656 Input VSYNC |
| | In/Out | DDC_SD_HMRX | HDMI Receiver DDC Data Channel This pin functions as the bi-directional data pin of the serial port to HDMI DDC receiver. This pin will require a pull-up 47 kΩ Resistor to the desired voltage level. |
| 10 | In | BT656_HS | BT656 Input HSYNC |
| | In | DDC_SC_HMRX | HDMI Receiver DDC Clock Channel This pin functions as the clock bus of the serial port to HDMI DDC receiver. This pin will require a pull-up 47 kΩ Resistor to the desired voltage level. |
| 11 | In | BT656_DE | BT656 Input DE |
| | Out | HPD_HMRX | HDMI Receiver HPD Output |
| 16 | In | RXCB_HMRX | HDMI Rx Negative Clock Channel |
| | In | BT656_D[0] | BT656 Input Data Bit 0 (LSB) |
| 17 | In | RXC_HMRX | HDMI Rx Positive Clock Channel |
| | In | BT656_D[1] | BT656 Input Data Bit 1 |
| 18 | In | RX0B_HMRX | HDMI Rx Negative Data Channel 0 |
| | In | BT656_D[2] | BT656 Input Data Bit 2 |
| 19 | In | RX0_HMRX | HDMI Rx Positive Data Channel 0 |
| | In | BT656_D[3] | BT656 Input Data Bit 3 |

| | | | |
|----|--------|-------------|--|
| 21 | In | RX1B_HMRX | HDMI Rx Negative Data Channel 1 |
| | In | BT656_D[4] | BT656 Input Data Bit 4 |
| 22 | In | RX1_HMRX | HDMI Rx Positive Data Channel 1 |
| | In | BT656_D[5] | BT656 Input Data Bit 5 |
| 24 | In | RX2B_HMRX | HDMI Rx Negative Data Channel 2 |
| | In | BT656_D[6] | BT656 Input Data Bit 6 |
| 25 | In | RX2_HMRX | HDMI Rx Positive Data Channel 2 |
| | In | BT656_D[7] | BT656 Input Data Bit 7 (MSB) |
| 30 | Out | TX1B_DPTX | DP Tx Lane 1 Negative Data |
| 31 | Out | TX1_DPTX | DP Tx Lane 1 Positive Data |
| 34 | Out | TX0B_DPTX | DP Tx Lane 0 Negative Data |
| 35 | Out | TX0_DPTX | DP Tx Lane 0 Positive Data |
| 39 | Out | VGA_VSO | VGA VSYNC Output |
| | In/Out | GPIO[7] | General Purpose Input/Output |
| 40 | Out | VGA_HSO | VGA HSYNC Output |
| | In/Out | GPIO[6] | General Purpose Input/Output |
| 41 | In | I2SRX_WS | WS of I2S Audio Input |
| | In/Out | GPIOL[2] | General Purpose Input/Output Default definition is backlight brightness control |
| 42 | In | SPDIF_RX | SPDIF Audio Input |
| | In | I2SDATA_RX | Data of I2S Audio Input |
| | In/Out | GPIOL[1] | General Purpose Input/Output |
| 43 | In | I2SRX_CLK | Input Clock of I2S Audio Input |
| | In/Out | GPIOL[3] | General Purpose Input/Output |
| 44 | In/Out | GPIOL[0] | General Purpose Input/Output |
| 46 | In | RSTB | Chip Reset Low to 0V for reset. Typical High level is 3.3V |
| 47 | In/Out | DDC_SD_LDTX | LVDS Transmitter DDC Data Channel This pin functions as the bi-directional data pin of the serial port to LVDS DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. |
| 48 | Out | DDC_SC_LDTX | LVDS Transmitter DDC Clock Channel This pin functions as the clock bus of the serial port to LVDS DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. |
| 51 | Out | TTLTX_HS | TTL Transmitter HSYNC Output |
| | In/Out | LVDS CG[1] | General Purpose Input/Output Default definition is LVDS Panel Selection control |
| | Out | VGA_HSYNC | VGA HSYNC Output |
| 52 | Out | TTLTX_VS | TTL Transmitter VSYNC Output |
| | In/Out | LVDS CG[0] | General Purpose Input/Output Default definition is LVDS Panel Selection control |
| | Out | VGA_VSYNC | VGA VSYNC Output |
| 53 | Out | TTLTX_DE | TTL Transmitter DE Output |

| | | | |
|----|--------|-------------|---|
| | In/Out | PWM_LDTX | LVDS Transmitter PWM Output |
| 54 | Out | TTLTX_D[0] | TTL Transmitter Data Bit 0 |
| | In/Out | ENPWR_LDTX | LVDS Panel Power Enable Output |
| 55 | Out | TTLTX_D[1] | TTL Transmitter Data Bit 1 |
| | Out | TXC2_LDTX | LVDS Transmitter Positive Even Clock Channel |
| 56 | Out | TTLTX_D[2] | TTL Transmitter Data Bit 2 |
| | Out | TXC2B_LDTX | LVDS Transmitter Negative Even Clock Channel |
| 57 | Out | TTLTX_D[3] | TTL Transmitter Data Bit 3 |
| | Out | TX7_LDTX | LVDS Transmitter Positive Even Data Channel 3 |
| 58 | Out | TTLTX_D[4] | TTL Transmitter Data Bit 4 |
| | Out | TX7B_LDTX | LVDS Transmitter Negative Even Data Channel 3 |
| 59 | Out | TTLTX_D[5] | TTL Transmitter Data Bit 5 |
| | Out | TX6_LDTX | LVDS Transmitter Positive Even Data Channel 2 |
| 60 | Out | TTLTX_D[6] | TTL Transmitter Data Bit 6 |
| | Out | TX6B_LDTX | LVDS Transmitter Negative Even Data Channel 2 |
| 61 | Out | TTLTX_D[7] | TTL Transmitter Data Bit 7 |
| | Out | TX5_LDTX | LVDS Transmitter Positive Even Data Channel 1 |
| 62 | Out | TTLTX_D[8] | TTL Transmitter Data Bit 8 |
| | Out | TX5B_LDTX | LVDS Transmitter Negative Even Data Channel 1 |
| 63 | Out | TTLTX_D[9] | TTL Transmitter Data Bit 9 |
| | Out | TX4_LDTX | LVDS Transmitter Positive Even Data Channel 0 |
| 64 | Out | TTLTX_CLKO | TTL Transmitter Clock Output |
| | Out | TX4B_LDTX | LVDS Transmitter Negative Even Data Channel 0 |
| 70 | Out | TTLTX_D[10] | TTL Transmitter Data Bit 10 |
| | Out | TXC1_LDTX | LVDS Transmitter Positive Odd Clock Channel |
| 71 | Out | TTLTX_D[11] | TTL Transmitter Data Bit 11 |
| | Out | TXC1B_LDTX | LVDS Transmitter Negative Odd Clock Channel |
| 72 | Out | TTLTX_D[12] | TTL Transmitter Data Bit 12 |
| | Out | TX3_LDTX | LVDS Transmitter Positive Odd Data Channel 3 |
| 73 | Out | TTLTX_D[13] | TTL Transmitter Data Bit 13 |
| | Out | TX3B_LDTX | LVDS Transmitter Negative Odd Data Channel 3 |
| 74 | Out | TTLTX_D[14] | TTL Transmitter Data Bit 14 |
| | Out | TX2_LDTX | LVDS Transmitter Positive Odd Data Channel 2 |
| 75 | Out | TTLTX_D[15] | TTL Transmitter Data Bit 15 |
| | Out | TX2B_LDTX | LVDS Transmitter Negative Odd Data Channel 2 |
| 76 | Out | TTLTX_D[16] | TTL Transmitter Data Bit 16 |
| | Out | TX1_LDTX | LVDS Transmitter Positive Odd Data Channel 1 |
| 77 | Out | TTLTX_D[17] | TTL Transmitter Data Bit 17 |
| | Out | TX1B_LDTX | LVDS Transmitter Negative Odd Data Channel 1 |

| | | | |
|----|--------|-------------|--|
| 78 | Out | TTLTX_D[18] | TTL Transmitter Data Bit 18 |
| | Out | TX0_LDTX | LVDS Transmitter Positive Odd Data Channel 0 |
| 79 | Out | TTLTX_D[19] | TTL Transmitter Data Bit 19 |
| | Out | TX0B_LDTX | LVDS Transmitter Negative Odd Data Channel 0 |
| 80 | Out | TTLTX_D[20] | TTL Transmitter Data Bit 20 |
| | In/Out | STEREO_LRS | General Purpose Input/Output Default definition is Left/Right Eye Swap for 3D mode |
| 81 | Out | TTLTX_D[21] | TTL Transmitter Data Bit 21 |
| | In/Out | STEREO_LBLK | General Purpose Input/Output Default definition is Left Eye Backlight Enable for 3D mode |
| 82 | Out | TTLTX_D[22] | TTL Transmitter Data Bit 22 |
| | In/Out | STEREO_RBLK | General Purpose Input/Output Default definition is Right Eye Backlight Enable for 3D mode |
| 83 | Out | TTLTX_D[23] | TTL Transmitter Data Bit 23 |
| | In/Out | STEREO_LRE | General Purpose Input/Output Default definition is Left/Right Eye Indicator for 3D mode |
| 86 | In/Out | AUXN_DPTX | DP Tx AUX CH Negative Data |
| 87 | In/Out | AUXP_DPTX | DP Tx AUX CH Positive Data |
| 88 | In/Out | SPDM | I2C Master Serial Port Data If EEPROM is not included inside CH7039 then this pin functions as the bi-directional data pin of the serial port to chip firmware and HDCP Key EEPROM. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. A pull-low resistor 10 kΩ to ground if unused. If EEPROM is included inside CH7039 then this pin can be connected to Host I2C SC to burn EEPROM in production or in evaluation. |
| 89 | Out | SPCM | I2C Master Serial Port Clock If EEPROM is not included inside CH7039 then this pin functions as the clock bus of the serial port to chip firmware and HDCP Key EEPROM. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. A pull-low resistor 10 kΩ to ground if unused. If EEPROM is included inside CH7039 then this pin can be connected to Host I2C SC to burn EEPROM in production or in evaluation. |
| 91 | Out | DDC_SC_VGA | VGA DDC Clock Channel This pin functions as the clock output pin of the serial port to VGA DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. |
| 92 | In/Out | DDC_SD_VGA | VGA DDC Data Channel This pin functions as the bi-directional data pin of the serial port to VGA DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. |
| 93 | In | SPC | I2C Slave Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up 6.8 kΩ Resistor is required. |
| 94 | In/Out | SPD | I2C Slave Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 kΩ Resistor is required. |
| 95 | Out | HPD_DPRX | DisplayPort Receiver HPD Output |
| 98 | Out | HMTXCB | HDMI Transmitter Negative Clock Channel |
| 99 | Out | HMTXC | HDMI Transmitter Positive Clock Channel |

| | | | |
|-----|--------|---------------|--|
| 100 | Out | HMTX0B | HDMI Transmitter Negative Data 0 Channel |
| 101 | Out | HMTX0 | HDMI Transmitter Positive Data 0 Channel |
| 103 | Out | HMTX1B | HDMI Transmitter Negative Data 1 Channel |
| 104 | Out | HMTX1 | HDMI Transmitter Positive Data 1 Channel |
| 105 | Out | HMTX2B | HDMI Transmitter Negative Data 2 Channel |
| 106 | Out | HMTX2 | HDMI Transmitter Positive Data 2 Channel |
| 112 | In | DPRX0 | DisplayPort Receiver Positive Lane 0 |
| 113 | In | DPRX0B | DisplayPort Receiver Negative Lane 0 |
| 115 | In | DPRX1 | DisplayPort Receiver Positive Lane 1 |
| 116 | In | DPRX1B | DisplayPort Receiver Negative Lane 1 |
| 120 | Out | DAC2 | VGA DAC Output |
| 122 | Out | DAC1 | VGA DAC Output |
| 124 | Out | DAC0 | VGA DAC Output |
| 126 | Out | CVBS | CVBS Output |
| 127 | In | HPD_DPTX | DP Tx HPD Input |
| 132 | In | ISSET | VGA Output Current Set This pin sets the DAC current. A 1 kΩ, 1% tolerance resistor should be connected between this pin and ground using short and wide traces. |
| 134 | In | ATPG | ATPG Enable (Internally pull-low) Chip test pin. This pin should be pulled low with a 10 kΩ resistor in the application. |
| 136 | Out | I2STX_WS | WS of I2S Audio Output |
| | In/Out | GPIOR[2] | General Purpose Input/Output Default definition is backlight brightness control |
| 137 | Out | SPDIF_TX | SPDIF Audio Output |
| | Out | I2SDATA_TX | Data of I2S Audio Output |
| | In/Out | GPIOR[1] | General Purpose Input/Output |
| 138 | Out | I2STX_CLK | Input Clock of I2S Audio Output |
| | In/Out | GPIOR[3] | General Purpose Input/Output |
| 139 | Out | I2STX_MCLK | I2S Output Clock I2STX_MCLK can be configured to be 128/256/384*Fs CMOS level signal, typical 3.3 for high, 0 for low. |
| | In/Out | GPIOR[0] | General Purpose Input/Output |
| 140 | Out | DDC_SC_HMTX | HDMI Transmitter DDC Clock Channel This pin functions as the clock bus of the serial port to HDMI DDC receiver. This pin will require a pull-up 1.8 kΩ Resistor to the desired voltage level. |
| 141 | In/Out | DDC_SD_HMTX | HDMI Transmitter DDC Data Channel This pin functions as the bi-directional data pin of the serial port to HDMI DDC receiver. This pin will require a pull-up 1.8 kΩ Resistor to the desired voltage level. |
| 143 | In | TTLRX_DIN[23] | TTL Receiver Data Input Bit 23 |
| 144 | In | TTLRX_DIN[22] | TTL Receiver Data Input Bit 22 |
| 145 | In | TTLRX_DIN[21] | TTL Receiver Data Input Bit 21 |
| 146 | In | TTLRX_DIN[20] | TTL Receiver Data Input Bit 20 |

| | | | |
|-----|----|---------------|---|
| 147 | In | TTLRX_DIN[19] | TTL Receiver Data Input Bit 19 |
| 148 | In | TTLRX_DIN[18] | TTL Receiver Data Input Bit 18 |
| | In | LVDSRX1[0] | LVDS Receiver Positive Odd Data Channel 0 |
| 149 | In | TTLRX_DIN[17] | TTL Receiver Data Input Bit 17 |
| | In | LVDSRX1B[0] | LVDS Receiver Negative Odd Data Channel 0 |
| 150 | In | TTLRX_DIN[16] | TTL Receiver Data Input Bit 16 |
| | In | LVDSRX1[1] | LVDS Receiver Positive Odd Data Channel 1 |
| 151 | In | TTLRX_DIN[15] | TTL Receiver Data Input Bit 15 |
| | In | LVDSRX1B[1] | LVDS Receiver Negative Odd Data Channel 1 |
| 152 | In | TTLRX_DIN[14] | TTL Receiver Data Input Bit 14 |
| | In | LVDSRX1[2] | LVDS Receiver Positive Odd Data Channel 2 |
| 153 | In | TTLRX_DIN[13] | TTL Receiver Data Input Bit 13 |
| | In | LVDSRX1B[2] | LVDS Receiver Negative Odd Data Channel 2 |
| 154 | In | TTLRX_DIN[12] | TTL Receiver Data Input Bit 12 |
| | In | LVDSRX1_CK | LVDS Receiver Positive Odd Clock Channel |
| 155 | In | TTLRX_DIN[11] | TTL Receiver Data Input Bit 11 |
| | In | LVDSRX1_CKB | LVDS Receiver Negative Odd Clock Channel |
| 156 | In | TTLRX_DIN[10] | TTL Receiver Data Input Bit 10 |
| | In | LVDSRX1[3] | LVDS Receiver Positive Odd Data Channel 3 |
| 157 | In | TTLRX_DIN[9] | TTL Receiver Data Input Bit 9 |
| | In | LVDSRX1B[3] | LVDS Receiver Negative Odd Data Channel 3 |
| 160 | In | TTLRX_CLKIN | TTL Receiver Clock Input |
| | In | LVDSRX2[0] | LVDS Receiver Positive Even Data Channel 0 |
| 161 | In | TTLRX_DIN[8] | TTL Receiver Data Input Bit 8 |
| | In | LVDSRX2B[0] | LVDS Receiver Negative Even Data Channel 0 |
| 162 | In | TTLRX_DIN[7] | TTL Receiver Data Input Bit 7 |
| | In | LVDSRX2[1] | LVDS Receiver Positive Even Data Channel 1 |
| 163 | In | TTLRX_DIN[6] | TTL Receiver Data Input Bit 6 |
| | In | LVDSRX2B[1] | LVDS Receiver Negative Even Data Channel 1 |
| 164 | In | TTLRX_DIN[5] | TTL Receiver Data Input Bit 5 |
| | In | LVDSRX2[2] | LVDS Receiver Positive Even Data Channel 2 |
| 165 | In | TTLRX_DIN[4] | TTL Receiver Data Input Bit 4 |
| | In | LVDSRX2B[2] | LVDS Receiver Negative Even Data Channel 2 |
| 166 | In | TTLRX_DIN[3] | TTL Receiver Data Input Bit 3 |
| | In | LVDSRX2_CK | LVDS Receiver Positive Even Clock Channel |
| 167 | In | TTLRX_DIN[2] | TTL Receiver Data Input Bit 2 |
| | In | LVDSRX2_CKB | LVDS Receiver Negative Even Clock Channel |
| 168 | In | TTLRX_DIN[1] | TTL Receiver Data Input Bit 1 |
| | In | LVDSRX2[3] | LVDS Receiver Positive Even Data Channel 3 |

| | | | |
|---|--------|--------------|--|
| 169 | In | TTLRX_DIN[0] | TTL Receiver Data Input Bit 0 |
| | In | LVDSRX2B[3] | LVDS Receiver Negative Even Data Channel 3 |
| 171 | In | TTLRX_DE | TTL Receiver DE Input |
| | In | LVDSRX_PWM | General Purpose Input |
| 172 | In | TTLRX_VSYNC | TTL Receiver VSYNC Input |
| | In | LVDSRX_ENBLK | General Purpose Input |
| 173 | In | TTLRX_HSYNC | TTL Receiver HSYNC Input |
| | In | LVDSRX_ENPWR | General Purpose Input |
| 174 | In/Out | AUXN_RX | DisplayPort Receiver Negative AUX CH |
| 175 | In/Out | AUXP_RX | DisplayPort Receiver Positive AUX CH |
| 176 | In | XI | Crystal Input / External Reference Input A parallel resonance crystal should be attached between this pin and XO. An external 3.3V CMOS compatible clock can drive the XI Input. |
| 12,23,38,97,119,123,133 | Power | AVCC_33 | Analog Power Supply (3.3V) |
| 13,20,36,50,84,96,102,114,121,125,130,131,158 | Power | AVSS | Analog Ground |
| 14,15,26,33,37,49,85,111,117,129 | Power | AVCC_12 | Analog/DCORE Power Supply (1.2V) |
| 27,32,66,109,110 | Power | DVDD | Digital Power Supply (1.2V) |
| 28,29,68,107,108 | Power | DGND | Digital Ground |
| 65,67,69,142,159,170 | Power | AVCC_IO | LVDS /TTL Rx/Tx Analog Power Supply(1.8~3.3V) While for LVDS configure, the power supply should be 3.3V |

Table 2: BGA196 Pin Name Description

| Pin # | Type | Symbol | Description |
|-------|------|--------------|--|
| A1 | In | XI | Crystal Input / External Reference Input A parallel resonance crystal should be attached between this pin and XO. An external 3.3V CMOS compatible clock can drive the XI Input. |
| A3 | In | TTLRX_DIN[1] | TTL Receiver Data Input Bit 1 |
| | In | LVDSRX2[3] | LVDS Receiver Positive Even Data Channel 3 |
| A4 | In | TTLRX_DIN[3] | TTL Receiver Data Input Bit 3 |
| | In | LVDSRX2_CK | LVDS Receiver Positive Even Clock Channel |
| A5 | In | TTLRX_DIN[5] | TTL Receiver Data Input Bit 5 |
| | In | LVDSRX2[2] | LVDS Receiver Positive Even Data Channel 2 |

| | | | |
|-----|-----|---------------|---|
| A6 | In | TTLRX_DIN[7] | TTL Receiver Data Input Bit 7 |
| | In | LVDSRX2[1] | LVDS Receiver Positive Even Data Channel 1 |
| A7 | In | TTLRX_CLKIN | TTL Receiver Clock Input |
| | In | LVDSRX2[0] | LVDS Receiver Positive Even Data Channel 0 |
| A8 | In | TTLRX_DIN[10] | TTL Receiver Data Input Bit 10 |
| | In | LVDSRX1[3] | LVDS Receiver Positive Odd Data Channel 3 |
| A9 | In | TTLRX_DIN[12] | TTL Receiver Data Input Bit 12 |
| | In | LVDSRX1_CK | LVDS Receiver Positive Odd Clock Channel |
| A10 | In | TTLRX_DIN[14] | TTL Receiver Data Input Bit 14 |
| | In | LVDSRX1[2] | LVDS Receiver Positive Odd Data Channel 2 |
| A11 | In | TTLRX_DIN[16] | TTL Receiver Data Input Bit 16 |
| | In | LVDSRX1[1] | LVDS Receiver Positive Odd Data Channel 1 |
| A12 | In | TTLRX_DIN[18] | TTL Receiver Data Input Bit 18 |
| | In | LVDSRX1[0] | LVDS Receiver Positive Odd Data Channel 0 |
| A14 | In | ISET | VGA Output Current Set This pin sets the DAC current. A 1 k Ω , 1% tolerance resistor should be connected between this pin and ground using short and wide traces. |
| B1 | Out | XO | Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. |
| B2 | Out | HPD_DPRX | DisplayPort Receiver HPD Output |
| B3 | In | TTLRX_DIN[0] | TTL Receiver Data Input Bit 0 |
| | In | LVDSRX2B[3] | LVDS Receiver Negative Even Data Channel 3 |
| B4 | In | TTLRX_DIN[2] | TTL Receiver Data Input Bit 2 |
| | In | LVDSRX2_CKB | LVDS Receiver Negative Even Clock Channel |
| B5 | In | TTLRX_DIN[4] | TTL Receiver Data Input Bit 4 |
| | In | LVDSRX2B[2] | LVDS Receiver Negative Even Data Channel 2 |
| B6 | In | TTLRX_DIN[6] | TTL Receiver Data Input Bit 6 |
| | In | LVDSRX2B[1] | LVDS Receiver Negative Even Data Channel 1 |
| B7 | In | TTLRX_DIN[8] | TTL Receiver Data Input Bit 8 |
| | In | LVDSRX2B[0] | LVDS Receiver Negative Even Data Channel 0 |
| B8 | In | TTLRX_DIN[9] | TTL Receiver Data Input Bit 9 |
| | In | LVDSRX1B[3] | LVDS Receiver Negative Odd Data Channel 3 |
| B9 | In | TTLRX_DIN[11] | TTL Receiver Data Input Bit 11 |
| | In | LVDSRX1_CKB | LVDS Receiver Negative Odd Clock Channel |
| B10 | In | TTLRX_DIN[13] | TTL Receiver Data Input Bit 13 |
| | In | LVDSRX1B[2] | LVDS Receiver Negative Odd Data Channel 2 |
| B11 | In | TTLRX_DIN[15] | TTL Receiver Data Input Bit 15 |
| | In | LVDSRX1B[1] | LVDS Receiver Negative Odd Data Channel 1 |
| B12 | In | TTLRX_DIN[17] | TTL Receiver Data Input Bit 17 |

| | | | |
|-----|--------|---------------|--|
| | In | LVDSRX1B[0] | LVDS Receiver Negative Odd Data Channel 0 |
| C3 | In/Out | GPIO[1] | General Purpose Input/Output |
| C4 | In | TTLRX_HSYNC | TTL Receiver HSYNC Input |
| | In | LVDSRX_ENPWR | General Purpose Input |
| C5 | In | TTLRX_VSYNC | TTL Receiver VSYNC Input |
| | In | LVDSRX_ENBLK | General Purpose Input |
| C6 | In | TTLRX_DE | TTL Receiver DE Input |
| | In | LVDSRX_PWM | General Purpose Input |
| C10 | In | TTLRX_DIN[21] | TTL Receiver Data Input Bit 21 |
| C11 | In | TTLRX_DIN[22] | TTL Receiver Data Input Bit 22 |
| C12 | In | TTLRX_DIN[23] | TTL Receiver Data Input Bit 23 |
| C13 | Out | CVBS | CVBS Output |
| C14 | Out | DAC0 | DAC Output |
| D1 | In | RXC_HMRX | HDMI Receiver Positive Clock Channel |
| | In | BT656_D[1] | BT656 Input Data Bit 1 |
| D2 | In | RXCB_HMRX | HDMI Receiver Negative Clock Channel |
| | In | BT656_D[0] | BT656 Input Data Bit 0 (LSB) |
| D3 | In | AS | Serial Port Slave Device Address Selection |
| D4 | In/Out | IRQ | General Purpose Input/Output Default definition is interrupt to CH7039 Host |
| D5 | In/Out | AUXP_RX | DisplayPort Receiver Positive AUX CH |
| D6 | In/Out | AUXN_RX | DisplayPort Receiver Negative AUX CH |
| D9 | In | TTLRX_DIN[19] | TTL Receiver Data Input Bit 19 |
| D10 | In | TTLRX_DIN[20] | TTL Receiver Data Input Bit 20 |
| D11 | Out | I2S_WSO | I2S Output Channel Select CMOS level signal, typical 3.3 for high, 0 for low. |
| D12 | In | HPD_DPTX | DisplayPort Transmitter HPD Input |
| D13 | Out | DAC1 | DAC Output |
| D14 | Out | DAC2 | DAC Output |
| E1 | In | RX0_HMRX | HDMI Receiver Positive Data Channel 0 |
| | In | BT656_D[3] | BT656 Input Data Bit 3 |
| E2 | In | RX0B_HMRX | HDMI Receiver Negative Data Channel 0 |
| | In | BT656_D[2] | BT656 Input Data Bit 2 |
| E3 | In | AVSS_PLL | Analog ground |
| E4 | In | BT656_VS | BT656 Input VSYNC |
| | In/Out | DDC_SD_HMRX | HDMI Receiver DDC Data Channel This pin functions as the bi-directional data pin of the serial port to HDMI DDC receiver. This pin will require a pull-up 47 kΩ Resistor to the desired voltage level. |
| E5 | IN | SDET_DPRX | DisplayPort Receiver Detection |
| E10 | Out | I2S_CLKO | I2S Output Clock CMOS level signal, typical 3.3 for high, 0 for low. |

| | | | |
|-----|--------|-------------|--|
| | In/Out | GPIOR[3] | General Purpose Input/Output |
| | Out | SPDIF_DO0 | SPDIF Data Output 0 for 8 CH mode |
| E11 | Out | I2S_DO | I2S Data Output for 2 CH mode or I2S Data Output 0 for 8 CH mode CMOS level signal, typical 3.3 for high, 0 for low. |
| | Out | SPDIF_DO | S/PDIF Data Output |
| | In/Out | GPIOR[1] | General Purpose Input/Output |
| E12 | In/Out | GPIO[5] | General Purpose Input/Output |
| F1 | In | RX1_HMRX | HDMI Receiver Positive Data Channel 1 |
| | In | BT656_D[5] | BT656 Input Data Bit 2 |
| F2 | In | RX1B_HMRX | HDMI Receiver Negative Data Channel 1 |
| | In | BT656_D[4] | BT656 Input Data Bit 3 |
| F3 | In | BT656_CLK | BT656 Input Clock |
| F4 | In | BT656_HS | BT656 Input HSYNC |
| | In | DDC_SC_HMRX | HDMI Receiver DDC Clock Channel This pin functions as the clock bus of the serial port to HDMI DDC receiver. This pin will require a pull-up 47 kΩ Resistor to the desired voltage level. |
| F6 | In | HPD_HMTX | HDMI Transmitter HPD Input |
| F7 | In/Out | DDC_SD_HMTX | HDMI Transmitter DDC Data Channel This pin functions as the bi-directional data pin of the serial port to HDMI DDC receiver. This pin will require a pull-up 1.8 kΩ Resistor to the desired voltage level. |
| F8 | Out | DDC_SC_HMTX | HDMI Transmitter DDC Clock Channel This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a pull-up 1.8 kΩ Resistor to the desired voltage level. |
| F9 | In | ATPG | ATPG Enable |
| F11 | Out | I2S_MCLKO | I2S Output Clock I2S_MCLKO can be configured to be 128/256/384*Fs CMOS level signal, typical 3.3 for high, 0 for low. |
| | In/Out | GPIOR[0] | General Purpose Input/Output |
| | Out | SPDIF_DO3 | SPDIF Data Output 3 for 8 CH mode (RevC Only) |
| F13 | In | DPRX1 | DisplayPort Receiver Positive Lane 1 |
| F14 | In | DPRX1B | DisplayPort Receiver Negative Lane 1 |
| G1 | In | RX2_HMRX | HDMI Receiver Positive Data Channel 2 |
| | In | BT656_D[7] | BT656 Input Data Bit 0 (MSB) |
| G2 | In | RX2B_HMRX | HDMI Receiver Negative Data Channel 2 |
| | In | BT656_D[6] | BT656 Input Data Bit 1 |
| G4 | In | BT656_DE | BT656 Input DE |
| | Out | HPD_HMRX | HDMI Receiver HPD Output |
| G6 | In | BDIC | Power Level Detection Pull Low to disable 3.3V power level detection; Pull High to enable 3.3V power level detection; |
| G9 | In/Out | GPIO[0] | General Purpose Input/Output |
| G11 | In/Out | GPIO[4] | General Purpose Input/Output |

| | | | |
|-----|--------|-------------|--|
| | Out | I2S_DO1 | I2S Data Output 1 for 8 CH mode |
| G13 | In | DPRX0 | DisplayPort Receiver Positive Lane 0 |
| G14 | In | DPRX0B | DisplayPort Receiver Negative Lane 0 |
| H6 | In/Out | BLDN | General Purpose Input/Output Default definition is LCD backlight brightness control |
| H9 | In | RESETB | Chip Reset Low to 0V for reset. Typical High level is 3.3V |
| H11 | In/Out | SPD | I2C Slave Serial Port Data This pin functions as the data pin of the serial port. External pull-up 6.8 kΩ Resistor is required. |
| J1 | Out | TX1B_DPTX | DisplayPort Transmitter Lane 1 Negative Data |
| J2 | Out | TX1_DPTX | DisplayPort Transmitter Lane 1 Positive Data |
| J6 | In | CLK_I2SIN | Input Clock of I2S Input |
| | In/Out | GPIOL[3] | General Purpose Input/Output |
| J7 | In/Out | GPIO[2] | General Purpose Input/Output |
| J8 | In/Out | DDC_SD_LDTX | LVDS Transmitter DDC Data Channel This pin functions as the bi-directional data pin of the serial port to LVDS DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. |
| J9 | Out | DDC_SC_LDTX | LVDS Transmitter DDC Clock Channel This pin functions as the clock bus of the serial port to LVDS DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. |
| J13 | Out | HMTX2B | HDMI Transmitter Negative Data 2 Channel |
| J14 | Out | HMTX2 | HDMI Transmitter Positive Data 2 Channel |
| K1 | Out | TX0B_DPTX | DisplayPort Transmitter Lane 0 Negative Data |
| K2 | Out | TX0_DPTX | DisplayPort Transmitter Lane 0 Positive Data |
| K4 | Out | VGA_VSYNC | VGA VSYNC Output |
| | In/Out | GPIO[7] | General Purpose Input/Output |
| K5 | Out | VGA_HSYNC | VGA HSYNC Output |
| | In/Out | GPIO[6] | General Purpose Input/Output |
| K10 | In | SPC | I2C Slave Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up 6.8 kΩ Resistor is required. |
| K11 | In/Out | DDC_SD_VGA | VGA DDC Data Channel This pin functions as the bi-directional data pin of the serial port to VGA DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. |
| K13 | Out | HMTX1B | HDMI Transmitter Negative Data 1 Channel |
| K14 | Out | HMTX1 | HDMI Transmitter Positive Data 1 Channel |
| L5 | In | WS_I2SIN | WS of I2S Input |
| | In/Out | GPIOL[2] | General Purpose Input/Output |
| L6 | In | DATA_I2SIN | Data of I2S Input |
| | In | SPDIF_IN | SPDIF Input |
| | In/Out | GPIOL[1] | General Purpose Input/Output |
| L9 | In/Out | SPDM | I2C Master Serial Port Data If EEPROM is not included inside CH7039 then this pin functions |

| | | | |
|-----|--------|-------------|---|
| | | | as the bi-directional data pin of the serial port to chip firmware and HDCP Key EEPROM. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. A pull-low resistor 10 kΩ to ground if unused. If EEPROM is included inside CH7039 then this pin can be connected to Host I2C SC to burn EEPROM in production or in evaluation. |
| L10 | Out | SPCM | I2C Master Serial Port Clock If EEPROM is not included inside CH7039 then this pin functions as the clock bus of the serial port to chip firmware and HDCP Key EEPROM. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. A pull-low resistor 10 kΩ to ground if unused. If EEPROM is included inside CH7039 then this pin can be connected to Host I2C SC to burn EEPROM in production or in evaluation. |
| L11 | Out | DDC_SC_VGA | VGA DDC Clock Channel This pin functions as the clock bus of the serial port to VGA DDC receiver. This pin will require a pull-up 5.6 kΩ Resistor to the desired voltage level. |
| L13 | Out | HMTX0B | HDMI Transmitter Negative Data 0 Channel |
| L14 | Out | HMTX0 | HDMI Transmitter Positive Data 0 Channel |
| M2 | Out | TTLTX_HSYNC | TTL Transmitter DE Output |
| | Out | VGA_HSYNC | VGA HSYNC Output |
| | In/Out | LVDS CG[1] | General Purpose Input/Output Default definition is LVDS Panel Selection control |
| M3 | Out | TTLTX_VSYNC | TTL Transmitter VSYNC Output |
| | Out | VGA_VSYNC | VGA VSYNC Output |
| | In/Out | LVDS CG[0] | General Purpose Input/Output Default definition is LVDS Panel Selection control |
| M4 | Out | TTLTX_DE | TTL Transmitter VSYNC Output |
| | In/Out | PWM_LDTX | General Purpose Input/Output Default definition is LVDS Panel PWM |
| M5 | Out | TTLTX_D[0] | TTL Transmitter Data Bit 0 |
| | In/Out | ENPWR_LDTX | General Purpose Input/Output Default definition is LVDS Panel Power Enable |
| M8 | Out | TTLTX_D[20] | TTL Transmitter Data Bit 20 |
| | In/Out | STEREO_LRS | General Purpose Input/Output Default definition is Left/Right Eye Swap for 3D mode |
| M9 | Out | TTLTX_D[21] | TTL Transmitter Data Bit 21 |
| | In/Out | STEREO_LBLK | General Purpose Input/Output Default definition is Left Eye Backlight Enable for 3D mode |
| M10 | Out | TTLTX_D[22] | TTL Transmitter Data Bit 22 |
| | In/Out | STEREO_RBLK | General Purpose Input/Output Default definition is Right Eye Backlight Enable for 3D mode |
| M11 | Out | TTLTX_D[23] | TTL Transmitter Data Bit 23 |
| | In/Out | STEREO_LRE | General Purpose Input/Output Default definition is Left/Right Eye Indicator for 3D mode |
| M13 | Out | HMTXCB | HDMI Transmitter Negative Clock Channel |
| M14 | Out | HMTXC | HDMI Transmitter Positive Clock Channel |
| N1 | Out | TTLTX_D[1] | TTL Transmitter Data Bit 1 |

| | | | |
|-----|-----|-------------|---|
| | Out | TXC2_LDTX | LVDS Transmitter Positive Even Clock Channel |
| | Out | DSD_DO0 | DSD Audio (One Bit Audio) Output 0 |
| N2 | Out | TTLTX_D[3] | TTL Transmitter Data Bit 3 |
| | Out | TX7_LDTX | LVDS Transmitter Positive Even Data Channel 3 |
| | Out | DSD_DO2 | DSD Audio (One Bit Audio) Output 2 |
| N3 | Out | TTLTX_D[5] | TTL Transmitter Data Bit 5 |
| | Out | TX6_LDTX | LVDS Transmitter Positive Even Data Channel 2 |
| | Out | DSD_DO4 | DSD Audio (One Bit Audio) Output 4 |
| N4 | Out | TTLTX_D[7] | TTL Transmitter Data Bit 7 |
| | Out | TX5_LDTX | LVDS Transmitter Positive Even Data Channel 1 |
| | Out | DSD_DO6 | DSD Audio (One Bit Audio) Output 6 |
| N5 | Out | TTLTX_D[9] | TTL Transmitter Data Bit 9 |
| | Out | TX4_LDTX | LVDS Transmitter Positive Even Data Channel 0 |
| | Out | DSD_WS | DSD Audio (One Bit Audio) WS |
| N7 | Out | TTLTX_D[10] | TTL Transmitter Data Bit 10 |
| | Out | TXC1_LDTX | LVDS Transmitter Positive Odd Clock Channel |
| N8 | Out | TTLTX_D[12] | TTL Transmitter Data Bit 12 |
| | Out | TX3_LDTX | LVDS Transmitter Positive Odd Data Channel 3 |
| N9 | Out | TTLTX_D[14] | TTL Transmitter Data Bit 14 |
| | Out | TX2_LDTX | LVDS Transmitter Positive Odd Data Channel 2 |
| N10 | Out | TTLTX_D[16] | TTL Transmitter Data Bit 16 |
| | Out | TX1_LDTX | LVDS Transmitter Positive Odd Data Channel 1 |
| N11 | Out | TTLTX_D[18] | TTL Transmitter Data Bit 18 |
| | Out | TX0_LDTX | LVDS Transmitter Positive Odd Data Channel 0 |
| P1 | Out | TTLTX_D[2] | TTL Transmitter Data Bit 2 |
| | Out | TXC2B_LDTX | LVDS Transmitter Negative Even Clock Channel |
| | Out | DSD_DO1 | DSD Audio (One Bit Audio) Output 1 |
| P2 | Out | TTLTX_D[4] | TTL Transmitter Data Bit 4 |
| | Out | TX7B_LDTX | LVDS Transmitter Negative Even Data Channel 3 |
| | Out | DSD_DO3 | DSD Audio (One Bit Audio) Output 3 |
| P3 | Out | TTLTX_D[6] | TTL Transmitter Data Bit 6 |
| | Out | TX6B_LDTX | LVDS Transmitter Negative Even Data Channel 2 |
| | Out | DSD_DO5 | DSD Audio (One Bit Audio) Output 5 |
| P4 | Out | TTLTX_D[8] | TTL Transmitter Data Bit 8 |
| | Out | TX5B_LDTX | LVDS Transmitter Negative Even Data Channel 1 |
| | Out | DSD_DO7 | DSD Audio (One Bit Audio) Output 7 |
| P5 | Out | TTLTX_CLK | TTL Transmitter Clock Output |
| | Out | TX4B_LDTX | LVDS Transmitter Negative Even Data Channel 0 |
| | Out | DSD_CLK | DSD Bit Clock Output |

| | | | |
|--|--------|-------------|---|
| P7 | Out | TTLTX_D[11] | TTL Transmitter Data Bit 11 |
| | Out | TXC1B_LDTX | LVDS Transmitter Negative Odd Clock Channel |
| P8 | Out | TTLTX_D[13] | TTL Transmitter Data Bit 13 |
| | Out | TX3B_LDTX | LVDS Transmitter Negative Odd Data Channel 3 |
| P9 | Out | TTLTX_D[15] | TTL Transmitter Data Bit 15 |
| | Out | TX2B_LDTX | LVDS Transmitter Negative Odd Data Channel 2 |
| P10 | Out | TTLTX_D[17] | TTL Transmitter Data Bit 17 |
| | Out | TX1B_LDTX | LVDS Transmitter Negative Odd Data Channel 1 |
| P11 | Out | TTLTX_D[19] | TTL Transmitter Data Bit 19 |
| | Out | TX0B_LDTX | LVDS Transmitter Negative Odd Data Channel 0 |
| P12 | In/Out | AUXN_DPTX | DisplayPort Transmitter AUX CH Negative Data |
| P13 | In/Out | AUXP_DPTX | DisplayPort Transmitter AUX CH Positive Data |
| P14 | In/Out | GPIO[3] | General Purpose Input/Output |
| A2,B13, D8,M6, P6 | Power | AVCC_IO | LVDS /TTL Rx/Tx Analog Power Supply(1.8~3.3V) While for LVDS configure, the power supply should be 3.3V |
| A13,C2, F12,G12 ,J4,L12 | Power | AVCC_33 | Analog 3.3V Power Supply |
| B14,C9, E13,H1, H13,H1 4,L1,L2, L3,M1, M12,N1 2,N13 | Power | AVSS | Analog ground |
| C1,E14, K3,L4,N 14 | Power | AVCC_12 | Analog 1.2V Power Supply |
| C7,C8, D7,E6~ E9,F5,F 10,G5,G 7,G8,G1 0,H2~H 5,H7,H8 ,H10,J5, J10,J11, K6~K9, K12,L7, L8,M7 | Power | DGND | Digital Power Ground |
| G3,H12, J3,J12,N 6 | Power | DVDD | Digital Power Supply, 1.2V |

2.0 PACKAGE DIMENSION

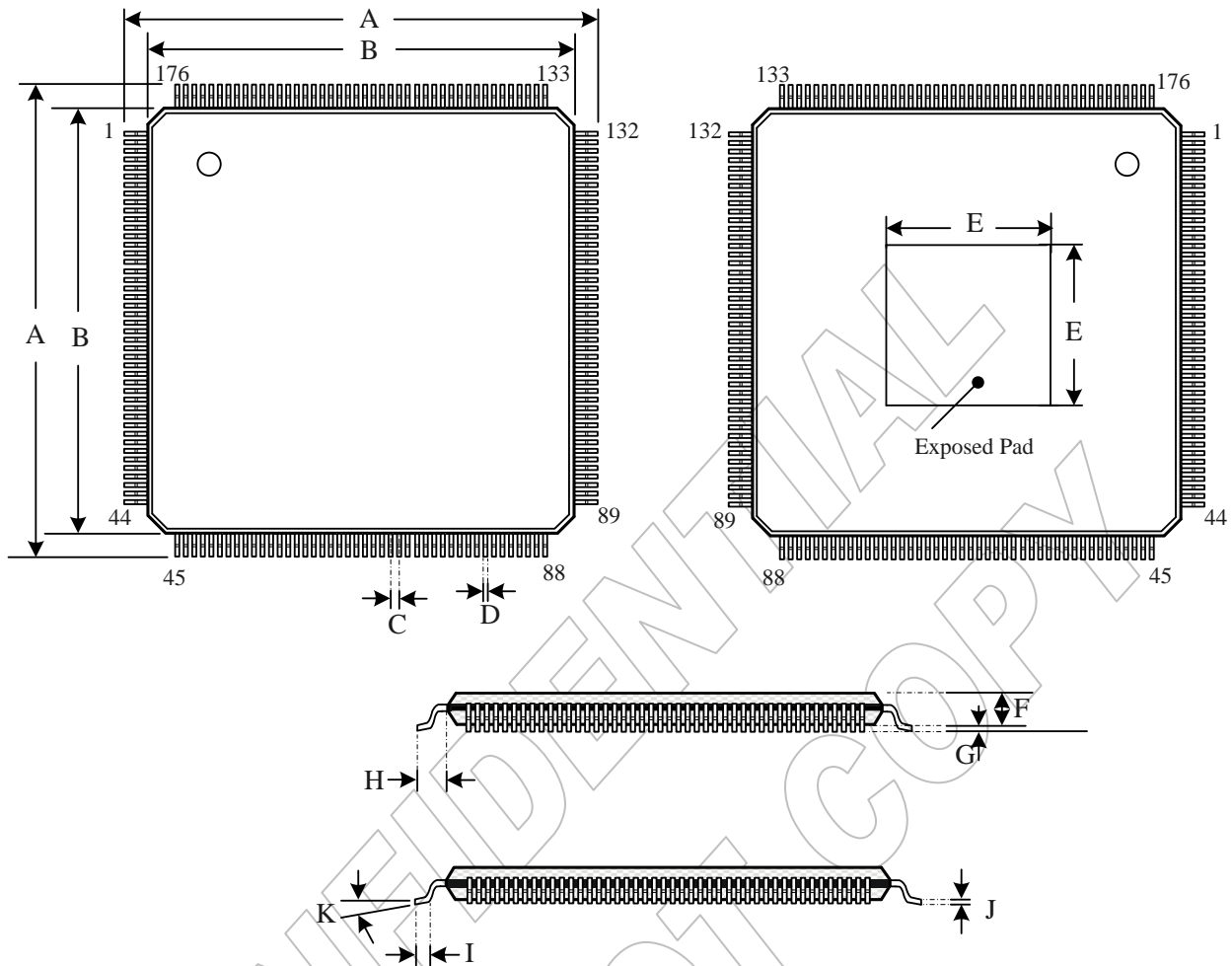


Figure 4: 176 pin LQFP package (20 x 20 mm)

Table of Dimensions

| No. of Leads | | SYMBOL | | | | | | | | | | |
|------------------|-----|--------|-------|------|------|------|------|------|------|------|------|------|
| 176 (20 X 20 mm) | | A | B | C | D | E | F | G | H | I | J | K |
| Milli-meters | MIN | 21.80 | 19.90 | 0.35 | 0.13 | 6.50 | 1.35 | 0.05 | 1.00 | 0.45 | 0.9 | 0° |
| | NOM | 22.00 | 20.00 | 0.40 | 0.18 | | 1.40 | - | | 0.60 | - | 3.5° |
| | MAX | 22.20 | 20.10 | 0.45 | 0.23 | | 1.45 | 0.15 | | 0.75 | 0.20 | 7° |

Notes:

Conforms to JEDEC standard JESD-30 MO-220.

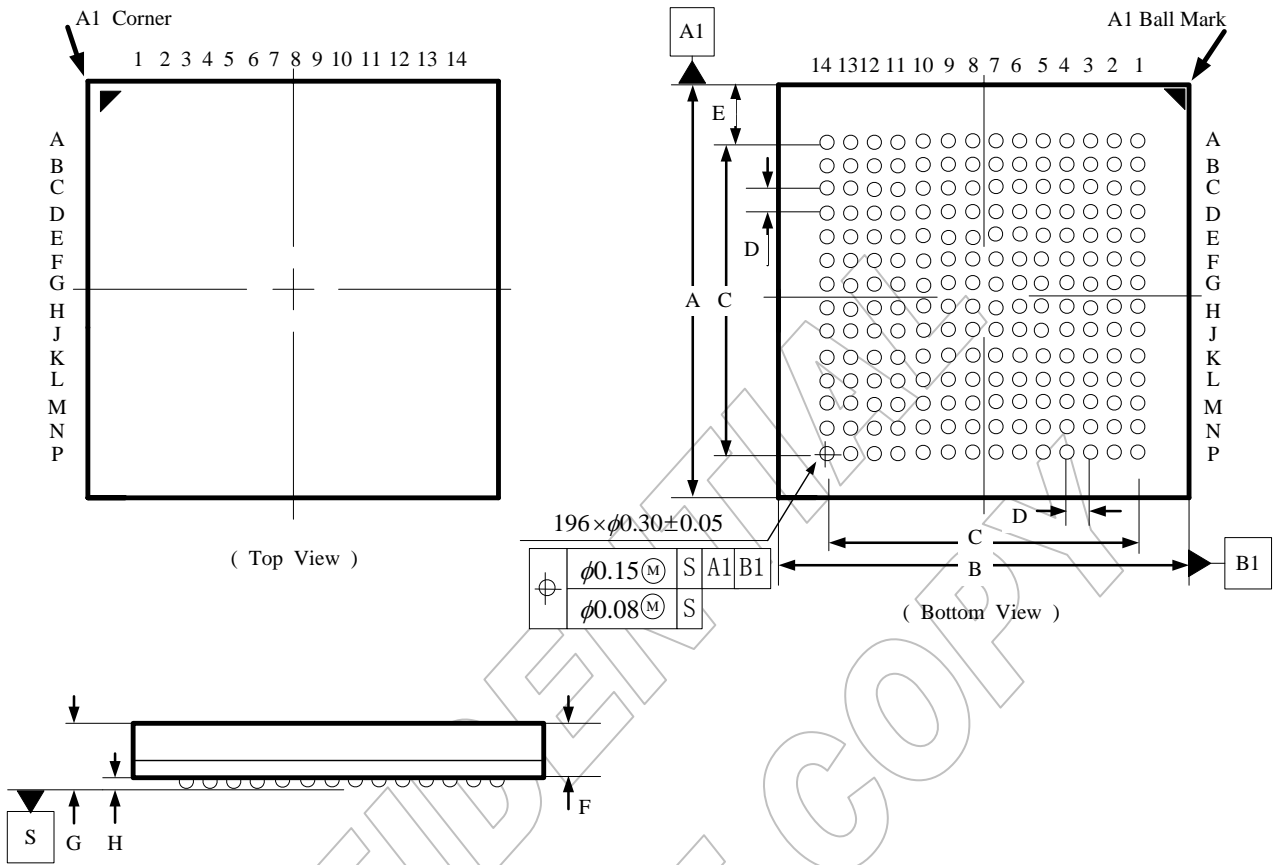


Figure 5: 196 Pin BGA Package (10x10 mm)

Table of Dimensions

| No. of Leads | | SYMBOL | | | | | | | |
|----------------|-----|--------|-------|------|------|-------------|------|------|------|
| 196 (10x10 mm) | | A | B | C | D | E | F | G | H |
| Milli-meters | MIN | 9.90 | 9.90 | 8.45 | 0.65 | 0.78 REF | 0.76 | - | 0.16 |
| | NOM | 10.00 | 10.00 | | | | 0.81 | - | 0.21 |
| | MAX | 10.10 | 10.10 | | | | 0.86 | 1.12 | 0.26 |

Notes:

1. All dimensions are in millimeters.
2. Solder ball dimension is post reflow diameter.

3.0 REVISION HISTORY

| Rev. # | Date | Section | Description |
|--------|------------|-------------------|------------------------------|
| 1.0 | 2016.02.03 | All | First Official Release |
| 1.1 | 2016.02.03 | Order Information | Update the Order Information |
| 1.11 | 2016.04.26 | 1.2 | Update the pin description |

CONFIDENTIAL
DO NOT COPY

Disclaimer

This document provides technical information for the user. Chrontel reserves the right to make changes at any time without notice to improve and supply the best possible product and is not responsible and does not assume any liability for misapplication or use outside the limits specified in this document. We provide no warranty for the use of our products and assume no liability for errors contained in this document. The customer should make sure that they have the most recent data sheet version. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Chrontel, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Chrontel PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF Chrontel. Life support systems are those intended to support or sustain life and whose failure to perform when used as directed can reasonably expect to result in personal injury or death.

| ORDERING INFORMATION | | | |
|-----------------------------|----------------------|------------------------------------|-------------------------------|
| Part Number | Package Type | Operating Temperature Range | Minimum Order Quantity |
| CH7039A-TF | 176 ETQFP, Lead-free | Commercial : 0°C to 70°C | 60/Tray |
| CH7039A-GF | 196 BGA, Lead-free | Commercial : 0 to 70°C | 184/Tray |

Chrontel

Chrontel International Limited

129 Front Street, 5th floor,
 Hamilton, Bermuda HM12
www.chrontel.com
 E-mail: sales@chrontel.com