VC0738
Brief Data Sheet

Revision 1.1

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Revision Table				
Date	Rev.	Author	Content of revision	Approval
2014-4-1	0.10	Wan Hongxing	The initial version	
2014-4-29	0.20	Wan Hongxing	Update Ball function description	
2014-7-25	0.21	Wan Hongxing	Update Feature List	
2014-11-1	0.22	Wan Hongxing	Update POD	
2015-9-6	1.1	Wan Hongxing	Release Version	

Contents

1 Introduction

1.1 Overview

The Vimicro VC0738 is a multimedia processing SoC which is dedicated to the application of digital video surveillance system, which integrates ARM9 processor, a hardware H.264 video codec, a 2D graphics engine, some storage interfaces and many peripheral interfaces.

VC0738 supports H.264 encoding which may be two channels with full HD 1080P@60fps, eight channels with 720P@20fps, or maximum to eight channels SD(D1 or 960H)@25fps, or 16 channels CIF@25fps. At the same time, the integration of H.264 decoder can support one 1080P@60fps, or 4 channels 720P/SD(D1 or 960H)@25fps, or 16 channels CIF@25fps decoding.

Through the integration of 10M/100M Ethernet MAC with integrated Ethernet PHY, VC0738 can be connected to the Ethernet to realize the transmission and control of communications and other functions of the video stream. VC0738 can also be connected to network through the USB, SDIO interface with WIFI or 3G interface module.

VC0738 integrate 2 SATA interfaces, which can be connected to the hard disk and other equipment to as storage of audio and video stream. VC0738 can also use a USB adapter, SDIO interface to connect to the SD card or other storage device.

Display and graphics engine of VC0738 can support full HD resolution of 1920X1080, and also support integration of HDMI, VGA, CVBS, LCD and other video output interface circuit.

VC0738 external 16/32bits DDR3 is compatible with JEDEC standard, which support data rates of up to 1600 Mb/s (800 MHz) in TSMC 55GP.

As a high performance, high integration SOC, VC0738 is used mainly for the DVR. And also meet a simple scene HD IPC application and NVR application

1.2 Typical Applications:

The VC0738 is a professional high-end system-on-chip (SoC) designed for multi-channel 960H/D1 and high-definition (HD) digital video recorders (DVRs) and network video recorders (NVRs).With a high-performance ARM926 processor, an

engine supporting up to 8-channel D1/16-channels CIF real-time encoding and decoding, the VC0738 meets the rising demand for HD and network applications. The VC0738 also provides an outstanding video engine, various encoding/decoding algorithms, and multi-channel HD output capability.

These features guarantee users a high-quality image experience. In addition, the VC0738 supports various highly-integrated peripheral interfaces to meet customer requirements for functionality, features, and image quality, while reducing the engineering bill of material (EBOM) cost. The VC0738 is applicable to the following typical scenarios:

DVR

- DVR for 4xD1/960H@25fps+4xCIF/480H@25fps encoding + 4xD1/960H@25fps decoding
- DVR for 4x720P@25fps+4xD1@25fps encoding + 4x720P@25fps decoding
- DVR for 8xD1/960H@25fps+8xCIF/480H@25fps encoding + 4xD1/960H@25fps decoding
- DVR for 8x720P@20fps+8xD1@20fps encoding + 1x720P@20fps decoding
- DVR for 16xCIF@25fps encoding+16xQCIF@25fps encoding + 16xCIF@25fps decoding
- DVR for 16xD1@>20fps+16xCIF encoding + 16xD1@>20fps decoding

NVR

- NVR for 4xD1/4x960H@25fps decoding
- NVR for 4x720P@25fps decoding
- NVR for 1x1080P@60fps decoding

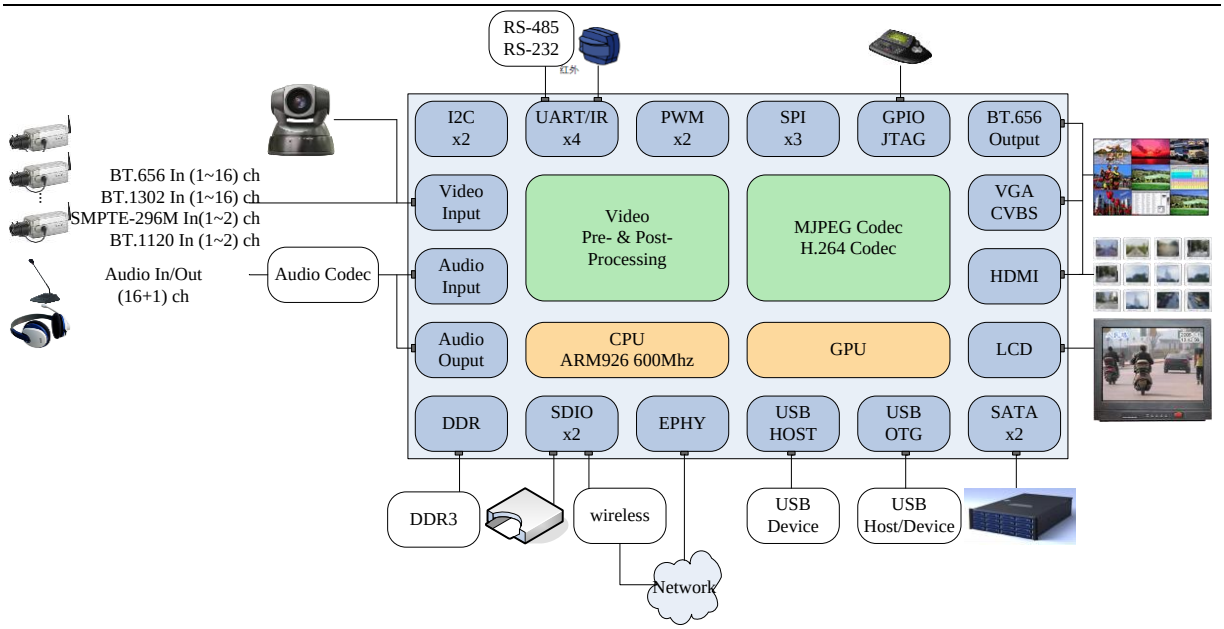
IPC

- IPC for 1x1080P@60fps real-time encoding

1.3 Key Specification

1.3.1 Overview

Figure 1-1 Show the logic block diagram



1.3.2 Process Core

The VC0738 uses the ARM926 with the maximum frequency 600MHz

- 16K Bytes I-cache and 16K Bytes D-cache
- 2 32bit Timer, each 32bit timer can be divided into 2 16bit timer

1.3.3 Video Encoding and Decoding Protocols

- H.264 Baseline Profile Level 4.2
- H.264 Main Profile Level 4.2
- H.264 High Profile Level 4.2
- MJPEG/JPEG Baseline

1.3.4 Video Encoding and Decoding

- H.264 encoding of multiple streams
  - No B frame support
  - 16xCIF@25fps + 16xQCIF@25fps
  - 4xD1@25fps + 4xCIF@25fps
  - 4x960H@25fps + 4x480H@25fps
  - 4x720P@25fps + 4xD1@25fps

- 8xD1@25fps + 8xCIF@25fps
- 8x720P@20fps + 8xD1@20fps
- 1x1080P@30fps+ 1xD1@30fps + 1xCIF@30fps
- 1x1080P@60fps with 1/2 pixel resolution
- CBR/VBR

- H.264 Decoding of multiple streams

  - No B frame support
  - 4xD1@25fps
  - 4x960H@25fps
  - 4x720P@25fps
  - 8xD1@25fps
  - 8x960H@25fps
  - 16xCIF@25fps
  - 1x1080P@60fps

- MJPEG/JPEG Encoding and Decoding

  - When recording with H.264, maximum support 1080P@5fps
  - When Only JPEG encoding, support maximum 5M@5fps
  - Decoding the same as encoding

1.3.5 Intelligent Video Analysis

- Motion detection
- Boundary security
- Video diagnosis
- Invisible watermark

1.3.6 Video and Graphic Processing

- Video pre- and post-processing, including frame dropping, lens cover detection, de-interlacing, image enhancement, edge enhancement, and 3D denoising
- Anti-flicker for output videos and graphics
- 1/64x to 16x video scaling
- 1/64x to 16x graphic scaling
- Flip/Mirror
- On-screen display (OSD) overlay of whole video or graphic layer before encoding
- POP
- Alpha blending of video layers and graphics layers

- Progressive conversion to interlaced (mainly used for standard BT656 and CVBS output)

1.3.7 Graphic engine

- Bit blit, stretch blit, pattern blit and fast clear
- Line drawing
- Rectangle fill and clear
- Mono expansion for text rendering
- Anti-aliased font support
- ROP2, ROP3, ROP4
- Alpha blending
- 90/180/270 degree rotation
- Vertical and Horizontal mirror
- Transparency by monochrome mask, chroma key or pattern mask
- High quality 9-tap filter for scaling
- 32K x 32K coordinate system
- Color space conversion between YUV and RGB for both BT709 and BT601
- Clipping window
- Color Index Input conversion Support
- Filter Blit
- Input Formats: (Only Filter Blit support YUV input)
  - A1R5G5B5
  - A4R4G4B4
  - A8R8G8B8
  - X1R5G5B5
  - X4R4G4B4
  - X8R8G8B8
  - RGB565
  - NV12 (semi-planer YUV420)
  - NV16 (semi-planer YUV422)
  - YUY2(package YUV422)
  - UYVY(package YUV422)
  - YV12(planer YUV420)
  - 8-bit color index
  - 1-bit monochrome
- The output data Formats:
  - A1R5G5B5
  - A4R4G4B4

- A8R8G8B8
- X1R5G5B5
- X4R4G4B4
- X8R8G8B8
- RGB565
- YUV422 interlaced

1.3.8 Audio Encoding and Decoding

- ADPCM,G711 and G726 hardware encoding with maximum 17 streams
- G723 and G729 software encoding
- Software decoding complying with various protocols

1.3.9 Video Interfaces

- Video input interfaces
  - 4xBT656@27/54/108MHz for 16 real-time inputs
  - 4x960H@36/72/144MHz for 16 real-time inputs
  - 2x720P@30fps/60fps for 2 real-time inputs (SMPTE-296M)
  - 4x720P@30fps for 8 real-time inputs (one port mulplex two 720P bitstream)
  - 2x1080P@148.5MHz for 2x1080P real-time inputs (one is DVP, one is BT1120)
- Video output interfaces
  - HDMI 1.3+VGA+CVBS outputs, The HDMI and VGA outputs can share the same source
  - 1xLCD and 1xBT656@27Mhz digital video output. The BT.656 and CVBS outputs share the same source
  - Maximum 1080P@60fps for HDMI or VGA
  - Graphics layers can support ARGB8888, RGB unpacked in 32bits, ARGB5555,RGB565 in 16bits, with the maximum resolution of 1920x1080

1.3.10 Audio Interfaces

The VC0738 has three inter-IC sound (I2S) interfaces. The details are as follows:

- Two for inputs
- One for output

- Audio format support 8bit/16bits sampling, the sampling rate are 8K,16K,32K and 48K
- Configurable master/slave mode

1.3.11 Ethernet Port

The VC0738 has one built-in megabit media access port. The details are as follows:

- MII mode
- 10/100 Mbit/s full-duplex or half-duplex mode
- Integrated EMAC PHY

1.3.12 SATA Port

The VC0738 has two SATA ports. The details are as follows

- Integrated SATA controller and PHY
- Two serial advanced technology attachment 2.6 (SATA2.6) interfaces. Maximum speed up to 3Gbps
- Support external SATA PM extended SATA equipment

1.3.13 USB Port

The VC0738 has two universal serial bus 2.0(USB2.0) ports. The details are as follows:

- Integrated USB2.0 controller + PHY
- One HOST
- One OTG

1.3.14 Peripherals

The VC0738 has the following peripheral interfaces:

- Four universal asynchronous receiver transmitter (UART) interfaces
- Two inter integrated circuit (I2C) interfaces
- Three serial peripheral (SPI) interfaces
- Two secure digital input/output 2.0 (SDIO2.0) interface
- Two pulse width modulation (PWM) interfaces
- Multiple general purpose input/output (GPIO) interfaces

1.3.15 Memory Interfaces

The VC0738 has the following memory interfaces:

- One external 16- or 32-bit DDR3 synchronous dynamic random access memory controller interface
  - Maximum frequency of 800Mhz
  - Support up to 512MB
  - One-die termination (ODT)
  - Automatic power consumption control
- SPI NOR flash interfaces
  - 1 bit SPI NOR flash interfaces
    - ✓ Maximum capacity of 32 MB for CS
- Built-in 16KB BOOTROM and 32KB SRAM

1.3.16 Physical Specifications

- Power consumption
- 2.5 W maximum power consumption
- Multi-level power-saving control
- Operating voltage
- 1.0 V core voltage
- 3.3/2.8/2.5/1.8V I/O voltage and 5 V margin voltage
- 1.5 V DDR3 SDRAM interface voltage
- Operating temperature ranging from -20℃ to +85℃
- Package
- Wire bonding fine ball grid array 441 (FBGA441)
- Body pitch: 0.8 mm (0.031 in.)
- Body size: 19mm x 19 mm (0.75 in x 0.75 in.)

1.4 Boot Modes

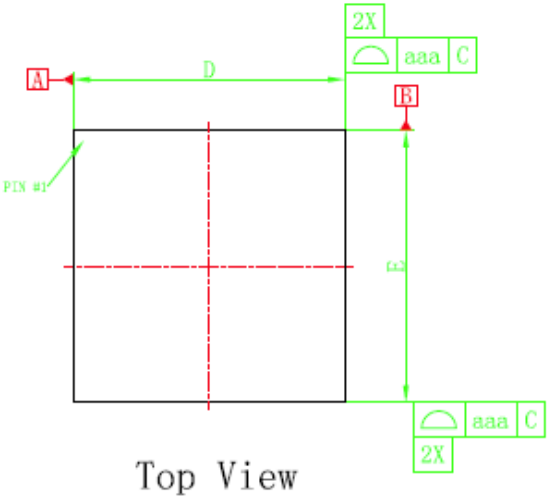
The VC0738 can boot from:

- BOOTROM as first level hardware boot
- SPI flash as second level software boot
- The debug interface (JTAG for boot code, UART, USB for OS debugging and applications)

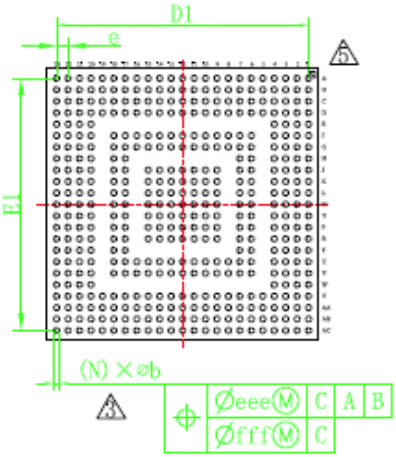
2 Hardware

2.1 Package and Pinout

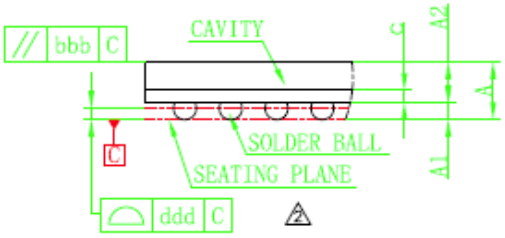
2.1.1 Package



Top View



Bottom View



DETAIL A

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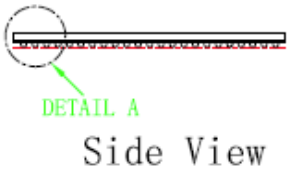

Side View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.310	—	—	0.052
A1	0.250	0.300	0.350	0.010	0.012	0.014
A2	0.860	0.910	0.960	0.034	0.036	0.038
c	0.170	0.210	0.250	0.007	0.008	0.010
D	18.900	19.000	19.100	0.744	0.748	0.752
E	18.900	19.000	19.100	0.744	0.748	0.752
D1	—	17.600	—	—	0.693	—
E1	—	17.600	—	—	0.693	—
e	—	0.800	—	—	0.031	—
b	0.350	0.400	0.450	0.014	0.016	0.018
aaa	0.150			0.006		
bbb	0.200			0.008		
ddd	0.100			0.004		
eee	0.150			0.006		
fff	0.080			0.003		
N	405			405		
MD/ME	23/23			23/23		

2.1.2 Pin Maps

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	UART0_RX	UART1_TX	DCVI0_DATA[7]	DCVI0_DATA[5]	DCVI0_DATA[3]	DCVI0_DATA[1]	DCVI0_CLK	DCVI1_CLK	DCVI1_DATA[7]	DCVI1_DATA[5]	DCVI1_DATA[3]
B	UART0_TX	UART0_CTSN	UART1_RX	DCVI0_DATA[6]	DCVI0_DATA[4]	DCVI0_DATA[2]	DCVI0_DATA[0]	VDD_IO_DCVI	VDD_IO_DCVI	DCVI1_DATA[6]	DCVI1_DATA[4]	DCVI1_DATA[2]
C	UART0_RTSN	I2S0_SDI	I2S0_SCLK	DCVI2_DATA[7]	DCVI2_DATA[5]	DCVI2_DATA[3]	DCVI2_DATA[1]	VDD_IO_DCVI	VDD_IO_DCVI	DCVI3_DATA[7]	DCVI3_DATA[5]	DCVI3_DATA[3]
D	I2C0_SCK	I2S01_MCLK	I2S2_MCLK	DCVI2_DATA[6]	DCVI2_DATA[4]	DCVI2_DATA[2]	DCVI2_DATA[0]	DCVI2_CLK	DCVI3_CLK	DCVI3_DATA[6]	DCVI3_DATA[4]	DCVI3_DATA[2]
E	I2C0_SDA	I2S0_WS	I2S2_SDO	I2S2_SCLK								
F	UOTG_DP	UOTG_DM	UOTG_VBUS	I2S2_WS		GPIO[5]	VDD_IO_LCD	VDD_IO_LCD	GPIO[7]	GPIO[9]	GPIO[11]	GPIO[13]
G	UHOST_DP	UHOST_DM	UOTG_ID	SPI0_SSN		GPIO[4]	VDD_IO_LCD	VDD_IO_LCD	GPIO[6]	GPIO[8]	GPIO[10]	GPIO[12]
H	TXN	TXP	TEST	SPI0_SCK		GPIO[3]	VDD_IO_SYS					
J	RXN	RXP	SPI0_MOSI	SPI0_MISO		VDD_IO_SYS	VDD_IO_SYS		GPIO[24]	GPIO[25]	GPIO[26]	GPIO[27]
K	VDD33_EPHY	VDD33_EPHY	UOTG_VSSA	UHOST_VDD33		VDD_IO_SYS	VSS		VSS	VSS	VSS	VSS
L	SATA_TXO_P	SATA_TXO_M	UOTG_RREFEX	VSS		UOTG_VDD33	VSS		VSS	VSS	VSS	VSS
M	VSS	SATA_RXO_M	UOTG_VSSAC	UHOST_RREFEXT		UHOST_VSSA	VSS		VSS	VSS	VSS	VSS

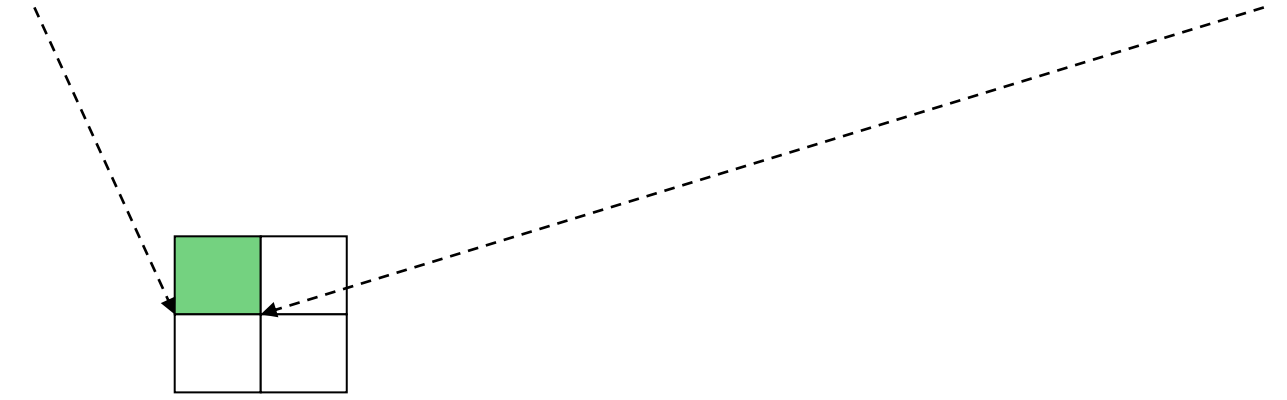

Figure 2-1 Pin Allocation of FBGA (left-top)

N	SATA_RX0_P	VSS	UHOST_VSSAC	VSS_EPHY		VSS	VSS		VSS	VDD_CORE	VDD_CORE	VDD_CORE
P	SATA_RX1_P	SATA_RX1_M	RTX	VSS_EPHY		SATA_REXT	VSS		VSS	VDD_CORE	VDD_CORE	VDD_CORE
R	VSS	SATA_TX1_M	SATA_VP25	SATA_VP25		VSS	VSS		VSS	VDD_CORE	VDD_CORE	VDD_CORE
T	SATA_TX1_P	VSS	SATA_VP25	SATA_VP25		VSS	VSS					
U	VDD_IO_DDR	VDD_IO_DDR	VDD_IO_DDR	VDD_IO_DDR		VDD_IO_DDR	VDD_IO_DDR	VSS	VSS	VDD_CORE	VDD_CORE	VDD_CORE
V	VDD_IO_DDR	VDD_IO_DDR	VDD_IO_DDR	VDD_IO_DDR		VDD_IO_DDR	VDD_IO_DDR	VDD_IO_DDR	VSS	VSS	DDR_PLL_VDD	DDR_PLL_VDD
W	DDR_A2	DDR_A13	VDD_IO_DDR	VDD_IO_DDR								
Y	DDR_A9	DDR_RSTN	VDD_IO_DDR	VDD_IO_DDR	VDD_IO_DDR	VSS	VSS	DDR_DQ22	DDR_DQ18	DDR_DM3	DDR_DQ29	DDR_DQS2_P
AA	DDR_A7	DDR_A5	VDD_IO_DDR	DDR_CASN	VDD_IO_DDR	VSS	VSS	DDR_DQ20	DDR_DQ16	DDR_DQ26	DDR_DQ28	DDR_DQ25
AB	DDR_A0	DDR_A3	DDR_BA2	DDR_ODT	DDR_DQ1	DDR_DQ3	VSS	DDR_DM1	DDR_DQ13	VSS	DDR_DQ15	DDR_DQS0_P
AC	VSS	DDR_BA0	DDR_CSN	DDR_WEN	DDR_RASN	VSS	DDR_DQ0	DDR_DQ2	VSS	DDR_DQ11	DDR_DQ9	VSS
	1	2	3	4	5	6	7	8	9	10	11	12

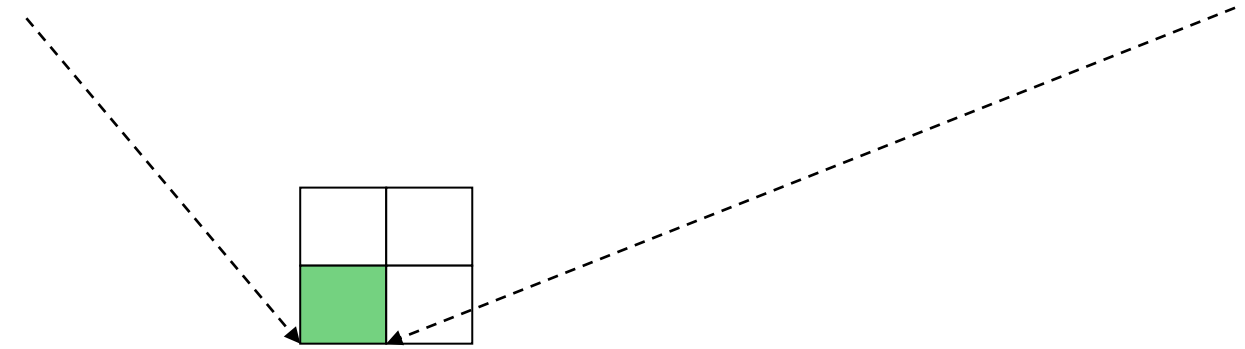

Figure 2-2 Pin Allocation of FBGA (left-bottom)

13	14	15	16	17	18	19	20	21	22	23	
DCVI1_DATA[1	AVDD33_HDMI	HDMI_RBIAS	AVSS33_ESD	AVDD33_ESD	HDMI_TX2N	HDMI_TX1N	HDMI_TXON	HDMI_TXCN	VDD_IO_SYS	VSS	A
DCVI1_DATA[0	VSS	AVSS33_HDMI	AVSS33_ESD	AVDD33_ESD	HDMI_TX2P	HDMI_TX1P	HDMI_TXOP	HDMI_TXCP	JTG_TCK	JTG_TDI	B
DCVI3_DATA[1	HDMI_VSS3IO	HDMI_CEC	HDMI_DSCL	HDMI_DSDA	HDMI_HPD	EMAC_COL	EMAC_RXDO	EMAC_RXD2	JTG_TMS	JTG_TDO	C
DCVI3_DATA[0	HDMI_VSS3IO	VDD_IO_HDMI	VDD_IO_LCD	VDD_IO_LCD	VSS	EMAC_CRS	EMAC_RXD1	EMAC_RXD3	JTG_RTCK	JTG_TRSTN	D
							EMAC_RXER	EMAC_TXDO	SDIOO_CMD	SDIOO_CLK	E
GPIO[15]	VDD_IO_LCD	GPIO[17]	GPIO[19]	GPIO[21]	GPIO[23]		GPIO[28]	SDIOO_DATA[3]	SDIOO_DATA[1]	SDIOO_DATA[0]	F
GPIO[14]	VDD_IO_LCD	GPIO[16]	GPIO[18]	GPIO[20]	GPIO[22]		GPIO[29]	RSTN	VSS	SDIOO_DATA[2]	G
				EMAC_RXDV	EMAC_TXD1		GPIO[30]	SDIOO_LOCKN	VDD_IO_SYS	VDD_IO_SYS	H
GPIO[0]	GPIO[1]	GPIO[2]		EMAC_TXD2	EMAC_TXD3		GPIO[31]	SDIOO_DETECTN	XCLKOUT	XCLKIN	J
VSS	VSS	VSS		EMAC_TXER	EMAC_TXEN		VDD_IO_SYS	VSSA_PLLO	VDDA_PLL1	VDDA_PLLO	K
VSS	VSS	VSS		EMAC_MDIO	EMAC_MDC		VGAO_HSYNC	VGA1_VSYNC	VDDA_PLL3	VDDA_PLL2	L
VSS	VSS	VSS		EMAC_RCK	EMAC_TCK		VGA1_HSYNC	VGAO_VSYNC	VSSA_PLL1	VSSA_PLL2	M

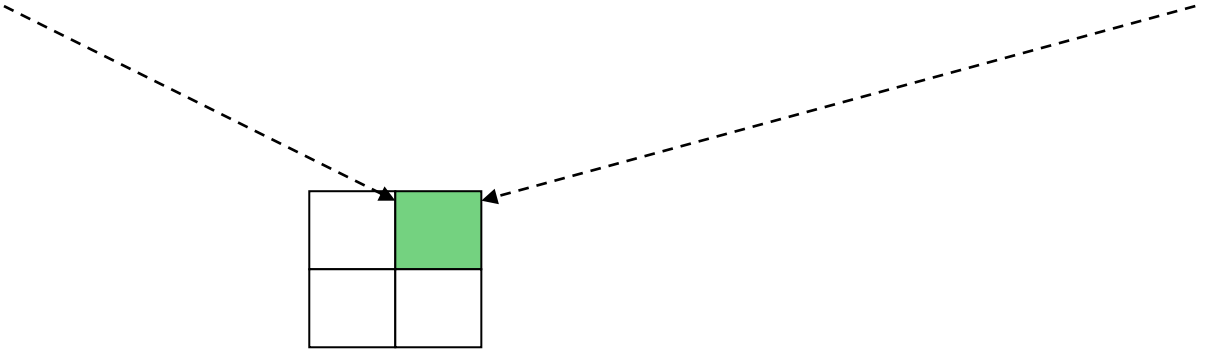

Figure 2-3 Pin Allocation of FBGA (right-top)

VDD_CORE	VDD_CORE	VDD_CORE		VDD_CORE	VSS		VSS	VDDA_PLL4	VSSA_PLL4	VSSA_PLL3	N
VDD_CORE	VDD_CORE	VDD_CORE		VDD_CORE	VDD_CORE		VDAC0_PGND1	VDAC0_PGND1	VDAC0_OUTP2	VDAC0_OUTP1	P
VDD_CORE	VDD_CORE	VDD_CORE		VDD_CORE	VDD_CORE		VDAC0_PVDD1	VDAC0_PVDD2	VDAC0_VDREF	VDAC0_OUTP0	R
				VDD_CORE	VDD_CORE		VDAC0_REXT	VDAC1_REXT	VDAC1_VDREF	VDAC1_OUTP0	T
VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE	VDD_CORE		VDAC1_PVDD1	VDAC1_PVDD2	VDAC1_OUTP2	VDAC1_OUTP1	U
DDR_PLL_VDD	DDR_PLL_VSS	DDR_PLL_VSS	DDR_PLL_VSS	DDR_DTO[0]	DDR_DTO[1]		VDAC1_PVDD1	VDAC1_PVDD1	DDR_A14	DDR_A1	V
							VDAC1_PGND1	VDAC1_PGND1	DDR_A8	DDR_A11	W
DDR_DQS3_P	DDR_DQ31	DDR_DQ30	DDR_DM2	DDR_DQ23	DDR_DQ21	DDR_ZQ	VSS	DDR_VREF	DDR_A4	DDR_A6	Y
DDR_DQS2_N	DDR_DQS3_N	DDR_DQ24	DDR_DQ27	DDR_DQ17	DDR_DQ19	DDR_ATO	VSS	DDR_CKE	DDR_BA1	DDR_A12	AA
VSS	DDR_DQS1_N	DDR_DQ12	VSS	DDR_DQ14	DDR_DM0	VSS	DDR_DQ7	DDR_DQ5	DDR_CLK_N	DDR_A10	AB
DDR_DQS0_N	DDR_DQS1_P	VSS	DDR_DQ8	DDR_DQ10	VSS	DDR_DQ4	DDR_DQ6	VSS	DDR_CLK_P	VSS	AC
13	14	15	16	17	18	19	20	21	22	23	

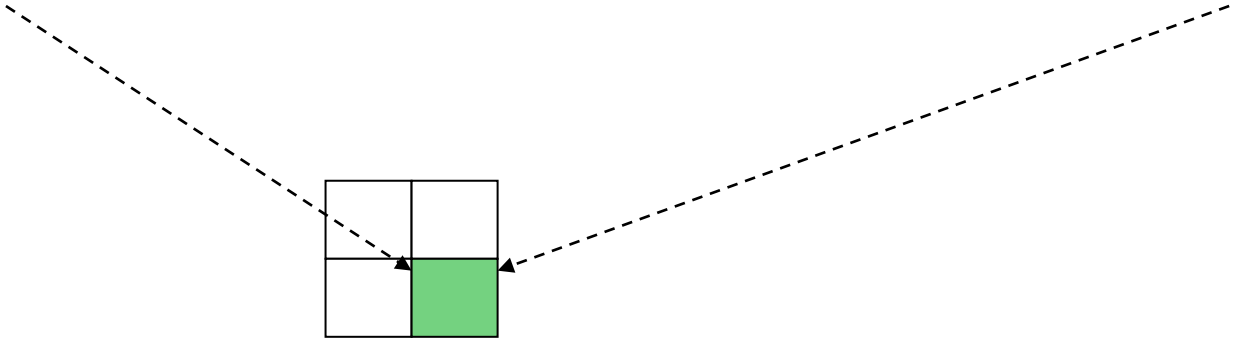

Figure 2-4 Pin Allocation of FBGA (right-bottom)

Table 2-1 Signal Description of VC0738

Pin Name	Pin No.	Pin Type	Drive Strength (mA)	I/O Power Or Range(v)	State After Reset Release	Pin Description
RSTN	**G21**	I,Sh	4mA	VDD_IO_SYS	I,RSTN	Reset Signal Input
XCLKIN	**J23**	I,Sh	4mA	VDD_IO_SYS	I,XCLKIN	External Crystal Input for System Clock
XCLKOUT	**J22**	O	4mA	VDD_IO_SYS	O,XCLKOUT	External Crystal Output for System Clock
TEST	**H3**	I,PD	4mA	VDD_IO_SYS	I,TEST	Test Mode Enable
JTG_TCK	**B22**	B,PD, Sh	4mA	VDD_IO_SYS	I,JTG_TCK, PD	JTAG Test Clock, share with LCD_DE, share with emacphy_padc_dpx_led, share with GPIO0[0]
JTG_TDI	**B23**	B,PD	4mA	VDD_IO_SYS	I,JTG_TDI,PD	JTAG Test Data Input, share with LCD_HSYNC, share with emacphy_padc_lnk_led, share with GPIO0[1]
JTG_TDO	**C23**	B,PD	4mA	VDD_IO_SYS	O,JTG_TDO ,PD	JTAG Test Data Output, share with LCD_VSYNC, share with emacphy_padc_spd_led, share with GPIO0[2]

JTG_TMS	**C22**	B,PD	8mA	VDD_IO_SYS	I,JTG_TMS,PD	JTAG Test Mode Select, share with LCD_PCLK, share with sata_p0_act_led, share with GPIO0[3]
JTG_TRSTN	**D23**	B,PU	4mA	VDD_IO_SYS	I,JTG_TRSTN,PU	JTAG Test Reset, active low, share with SDIO1_CLK, share with sata_p1_act_led, share with GPIO0[4]
JTG_RTCK	**D22**	B,PD	4mA	VDD_IO_SYS	O,JTG_RTCK,PD	PWM0 output, share with SDIO1_CMD, share with PWM0, share with GPIO0[5]
GPIO[0]	**J13**	B,PD	8mA	VDD_IO_LCD	I,GPIO[0],PD	GPIO[0], share with LCD_DATA[0], share with PWM1, share with UM_OUT[0]
GPIO[1]	**J14**	B,PD	8mA	VDD_IO_LCD	I,GPIO[1],PD	GPIO[1], share with LCD_DATA[1], share with UM_OUT[1]
GPIO[2]	**J15**	B,PD	8mA	VDD_IO_LCD	I,GPIO[2],PD	GPIO[2], share with LCD_DATA[2], share with UM_OUT[2]
GPIO[3]	**H6**	B,PD	8mA	VDD_IO_LCD	I,GPIO[3],PD	GPIO[3], share with LCD_DATA[3], share with UART2_TX, share with UM_OUT[3]
GPIO[4]	**G6**	B,PD	8mA	VDD_IO_LCD	I,GPIO[4],PD	GPIO[4], share with LCD_DATA[4], share with UART2_RX, share with UM_OUT[4]
GPIO[5]	**F6**	B,PD	8mA	VDD_IO_LCD	I,GPIO[5],PD	GPIO[5], share with LCD_DATA[5], share with UART3_TX, share with UM_OUT[5]
GPIO[6]	**G9**	B,PD	8mA	VDD_IO_LCD	I,GPIO[6],PD	GPIO[6], share with LCD_DATA[6], share with UART3_RX, share with UM_OUT[6]
GPIO[7]	**F9**	B,PD	8mA	VDD_IO_LCD	I,GPIO[7],PD	GPIO[7], share with LCD_DATA[7], share with SPI1_SCK, share with UM_OUT[7]
GPIO[8]	**G10**	B,PD	8mA	VDD_IO_LCD	I,GPIO[8],PD	GPIO[8], share with LCD_DATA[8], share with

						SPI1_SSN, share with UM_OUT[8]
GPIO[9]	**F10**	B,PD	8mA	VDD_IO_LCD	I,GPIO[9],PD	GPIO[9], share with LCD_DATA[9], share with SPI1_MOSI, share with UM_OUT[9]
GPIO[10]	**G11**	B,PD	8mA	VDD_IO_LCD	I,GPIO[10],PD	GPIO[10], share with LCD_DATA[10], share with SPI1_MISO, share with UM_OUT[10]
GPIO[11]	**F11**	B,PD	8mA	VDD_IO_LCD	I,GPIO[11],PD	GPIO[11], share with LCD_DATA[11], share with SPI2_SCK, share with UM_OUT[11]
GPIO[12]	**G12**	B,PD	8mA	VDD_IO_LCD	I,GPIO[12],PD	GPIO[12], share with LCD_DATA[12], share with SPI2_SSN, share with UM_OUT[12]
GPIO[13]	**F12**	B,PD	8mA	VDD_IO_LCD	I,GPIO[13],PD	GPIO[13], share with LCD_DATA[13], share with SPI2_MOSI, share with UM_OUT[13]
GPIO[14]	**G13**	B,PD	8mA	VDD_IO_LCD	I,GPIO[14],PD	GPIO[14], share with LCD_DATA[14], share with SPI2_MISO, share with UM_OUT[14]
GPIO[15]	**F13**	B,PD	8mA	VDD_IO_LCD	I,GPIO[15],PD	GPIO[15], share with LCD_DATA[15], share with UM_OUT[15]
GPIO[16]	**G15**	B,PD	8mA	VDD_IO_LCD	I,GPIO[16],PD	GPIO[16], share with LCD_DATA[16], share with UM_OUT[16]
GPIO[17]	**F15**	B,PD	8mA	VDD_IO_LCD	I,GPIO[17],PD	GPIO[17], share with LCD_DATA[17], share with I2S1_SCLK, share with UM_OUT[17]
GPIO[18]	**G16**	B,PD	8mA	VDD_IO_LCD	I,GPIO[18],PD	GPIO[18], share with LCD_DATA[18], share with I2S1_WS, share with UM_OUT[18]
GPIO[19]	**F16**	B,PD	8mA	VDD_IO_LCD	I,GPIO[19],PD	GPIO[19], share with LCD_DATA[19], share with

						I2S1_SDI, share with UM_OUT[19]
GPIO[20]	**G17**	B,PD	8mA	VDD_IO_LCD	I,GPIO[20],PD	GPIO[20], share with LCD_DATA[20], share with SATA_P0_CP_DET, share with UM_OUT[20]
GPIO[21]	**F17**	B,PD	8mA	VDD_IO_LCD	I,GPIO[21],PD	GPIO[21], share with LCD_DATA[21], share with SATA_P1_CP_DET, share with UM_OUT[21]
GPIO[22]	**G18**	B,PD	8mA	VDD_IO_LCD	I,GPIO[22],PD	GPIO[22], share with LCD_DATA[22], share with SATA_P0_CP_POD, share with UM_OUT[22]
GPIO[23]	**F18**	B,PD	8mA	VDD_IO_LCD	I,GPIO[23],PD	GPIO[23], share with LCD_DATA[23], share with SATA_P1_CP_POD, share with UM_OUT[23]
GPIO[24]	**J9**	B,PD	8mA	VDD_IO_DCVI	I,GPIO[24],PD	GPIO[24], share with SDIO0_DATA[4], share with SIF_PADC_CS_RSTN, share with UM_OUT[24]
GPIO[25]	**J10**	B,PD	8mA	VDD_IO_DCVI	I,GPIO[25],PD	GPIO[25], share with SDIO0_DATA[5], share with CLK_OUT1, share with UM_OUT[25]
GPIO[26]	**J11**	B,PD	8mA	VDD_IO_DCVI	I,GPIO[26],PD	GPIO[26], share with SDIO0_DATA[6], share with SIF_VSYNC, share with UM_OUT[26]
GPIO[27]	**J12**	B,PD	8mA	VDD_IO_DCVI	I,GPIO[27],PD	GPIO[27], share with SDIO0_DATA[7], share with SIF_HSYNC, share with UM_OUT[27]
GPIO[28]	**F20**	B,PD	8mA	VDD_IO_LCD	I,GPIO[28],PD	GPIO[28], share with SDIO1_DATA[0], share with I2C1_SCK, share with UM_OUT[28]
GPIO[29]	**G20**	B,PD	8mA	VDD_IO_LCD	I,GPIO[29],PD	GPIO[29], share with SDIO1_DATA[1], share with I2C1_SDA, share with UM_OUT[29]

GPIO[30]	**H20**	B,PD	8mA	VDD_IO_LCD	I,GPIO[30],PD	GPIO[30], share with SDIO1_DATA[2], share with UM_OUT[30]
GPIO[31]	**J20**	B,PD	8mA	VDD_IO_LCD	I,GPIO[31],PD	GPIO[31], share with SDIO1_DATA[3], share with UM_OUT[31]
I2C0_SCK	**D1**	B,Sh,PU	4mA	VDD_IO_SYS	I,GPIO0[6],PU	I2C0 Serial Clock, PULL UP IN PCB, share with GPIO0[6]
I2C0_SDA	**E1**	B,PU	4mA	VDD_IO_SYS	I,GPIO0[7],PU	I2C0 Serial Data, PULL UP IN PCB, share with GPIO0[7]
UART0_TX	**B1**	B,PD	4mA	VDD_IO_SYS	I,GPIO0[8],PD	UART0 Serial Transmit Port, share with GPIO0[8]
UART0_RX	**A2**	B,PU	4mA	VDD_IO_SYS	I,GPIO0[9],PU	UART0 Serial Receive Port, share with GPIO0[9]
UART0_RTSN	**C1**	B,PD	4mA	VDD_IO_SYS	I,GPIO0[10],PD	UART0 Request to Send, active low, share with GPIO0[10]
UART0_CTSN	**B2**	B,PU	4mA	VDD_IO_SYS	I,GPIO0[11],PU	UART0 Clear to Send, active low, share with GPIO0[11]
UART1_TX	**A3**	B,PD	4mA	VDD_IO_SYS	I,GPIO0[12],PD	UART0 Serial Transmit Port, share with GPIO0[12]
UART1_RX	**B3**	B,PU	4mA	VDD_IO_SYS	I,GPIO0[13],PU	UART0 Serial Receive Port, share with GPIO0[13]
SPI0_SCK	**H4**	B,Sh,PD	8mA	VDD_IO_SYS	I,GPIO0[14],PD	SPI0 Clock, share with GPIO0[14]
SPI0_SSN	**G4**	B,PD	8mA	VDD_IO_SYS	I,GPIO0[15],PD	SPI0 Slave Select, share with GPIO0[15]
SPI0_MOSI	**J3**	B,PD	8mA	VDD_IO_SYS	I,GPIO0[16],PD	SPI0 Master Output and Slave Input, share with GPIO0[16]
SPI0_MISO	**J4**	B,PD	8mA	VDD_IO_SYS	I,GPIO0[17],PD	SPI0 Master Input and Slave Output, share with GPIO0[17]
SDIO0_CLK	**E23**	B,Sh,PD	8mA	VDD_IO_SYS	I,GPIO0[18],PD	SDIO0 Clock , share with GPIO0[18]
SDIO0_CMD	**E22**	B,PD	8mA	VDD_IO_SYS	I,GPIO0[19],PD	SDIO0 Command/Response, share with GPIO0[19]
SDIO0_DATA[0]	**F23**	B,PD	8mA	VDD_IO_SYS	I,GPIO0[20],PD	SDIO0 Data 0, share with GPIO0[20]
SDIO0_DATA[1]	**F22**	B,PD	8mA	VDD_IO_SYS	I,GPIO0[21],PD	SDIO0 Data 1, share with GPIO0[21]
SDIO0_DATA[2]	**G23**	B,PD	8mA	VDD_IO_SYS	I,GPIO0[22],PD	SDIO0 Data 2, share with GPIO0[22]

SDIO0_DATA [3]	**F21**	B,PD	8mA	VDD_IO_SYS	I,GPIO0[23], PD	SDIO0 Data 3, share with GPIO0[23]
SDIO0_LOCKN	**H21**	B,PU	8mA	VDD_IO_SYS	I,GPIO0[24], PU	SDIO0 write protect of card socket, share with CLK_OUT0, share with GPIO0[24]
SDIO0_DETECTN	**J21**	B,PU	8mA	VDD_IO_SYS	I,GPIO0[25], PU	SDIO0 card-detection of card socket, share with GPIO0[25]
DCVI0_CLK	**A8**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[0],PU	1st port video input clock, share with SIF_PCLK, share with GPIO2[0]
DCVI0_DATA [0]	**B7**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[1],PU	1st port video input data 0, share with SIF_DATA[0], share with GPIO2[1]
DCVI0_DATA [1]	**A7**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[2],PU	1st port video input data 1, share with SIF_DATA[1], share with GPIO2[2]
DCVI0_DATA [2]	**B6**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[3],PU	1st port video input data 2, share with SIF_DATA[2], share with GPIO2[3]
DCVI0_DATA [3]	**A6**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[4],PU	1st port video input data 3, share with SIF_DATA[3], share with GPIO2[4]
DCVI0_DATA [4]	**B5**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[5],PU	1st port video input data 4, share with SIF_DATA[4], share with GPIO2[5]
DCVI0_DATA [5]	**A5**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[6],PU	1st port video input data 5, share with SIF_DATA[5], share with GPIO2[6]
DCVI0_DATA [6]	**B4**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[7],PU	1st port video input data 6, share with SIF_DATA[6], share with GPIO2[7]
DCVI0_DATA [7]	**A4**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[8],PU	1st port video input data 7, share with SIF_DATA[7], share with GPIO2[8]
DCVI1_CLK	**A9**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[9],PU	2nd port video input clock, share with SIF_PADC_CS_PWDN, share with GPIO2[9]
DCVI1_DATA [0]	**B13**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[10], PU	2nd port video input data 0, share with SIF_DATA[8], share with GPIO2[10]
DCVI1_DATA [1]	**A13**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[11], PU	2nd port video input data 1, share with SIF_DATA[9], share with

						GPIO2[11]
DCVI1_DATA [2]	**B12**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[12], PU	2nd port video input data 2, share with SIF_DATA[10], share with GPIO2[12]
DCVI1_DATA [3]	**A12**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[13], PU	2nd port video input data 3, share with SIF_DATA[11], share with GPIO2[13]
DCVI1_DATA [4]	**B11**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[14], PU	2nd port video input data 4, share with SIF_DATA[12], share with GPIO2[14]
DCVI1_DATA [5]	**A11**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[15], PU	2nd port video input data 5, share with SIF_DATA[13], share with GPIO2[15]
DCVI1_DATA [6]	**B10**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[16], PU	2nd port video input data 6, share with SIF_DATA[14], share with GPIO2[16]
DCVI1_DATA [7]	**A10**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[17], PU	2nd port video input data 7, share with SIF_DATA[15], share with GPIO2[17]
DCVI2_CLK	**D8**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[18], PU	3rd port video input clock, share with GPIO2[18]
DCVI2_DATA [0]	**D7**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[19], PU	3rd port video input data 0, share with GPIO2[19]
DCVI2_DATA [1]	**C7**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[20], PU	3rd port video input data 1, share with GPIO2[20]
DCVI2_DATA [2]	**D6**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[21], PU	3rd port video input data 2, share with GPIO2[21]
DCVI2_DATA [3]	**C6**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[22], PU	3rd port video input data 3, share with GPIO2[22]
DCVI2_DATA [4]	**D5**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[23], PU	3rd port video input data 4, share with GPIO2[23]
DCVI2_DATA [5]	**C5**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[24], PU	3rd port video input data 5, share with GPIO2[24]
DCVI2_DATA [6]	**D4**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[25], PU	3rd port video input data 6, share with GPIO2[25]
DCVI2_DATA [7]	**C4**	B,PU	4mA	VDD_IO_DCVI	I,GPIO2[26], PU	3rd port video input data 7, share with GPIO2[26]
DCVI3_CLK	**D9**	B,PU	4mA	VDD_IO_DCVI	I,GPIO3[0],PU	4th port video input clock, share with GPIO3[0]
DCVI3_DATA [0]	**D13**	B,PU	4mA	VDD_IO_DCVI	I,GPIO3[1],PU	4th port video input data 0, share with GPIO3[1]

DCVI3_DATA [1]	**C13**	B,PU	4mA	VDD_IO_DCVI	I,GPIO3[2],PU	4th port video input data 1, share with GPIO3[2]
DCVI3_DATA [2]	**D12**	B,PU	4mA	VDD_IO_DCVI	I,GPIO3[3],PU	4th port video input data 2, share with GPIO3[3]
DCVI3_DATA [3]	**C12**	B,PU	4mA	VDD_IO_DCVI	I,GPIO3[4],PU	4th port video input data 3, share with GPIO3[4]
DCVI3_DATA [4]	**D11**	B,PU	4mA	VDD_IO_DCVI	I,GPIO3[5],PU	4th port video input data 4, share with GPIO3[5]
DCVI3_DATA [5]	**C11**	B,PU	4mA	VDD_IO_DCVI	I,GPIO3[6],PU	4th port video input data 5, share with GPIO3[6]
DCVI3_DATA [6]	**D10**	B,PU	4mA	VDD_IO_DCVI	I,GPIO3[7],PU	4th port video input data 6, share with GPIO3[7]
DCVI3_DATA [7]	**C10**	B,PU	4mA	VDD_IO_DCVI	I,GPIO3[8],PU	4th port video input data 7, share with GPIO3[8]
I2S2_MCLK	**D3**	B,PD	8mA	VDD_IO_SYS	I,GPIO3[9],PD	Audio input0 Codec Master Clock, share with GPIO3[9]
I2S2_SCLK	**E4**	B,PD	8mA	VDD_IO_SYS	I,GPIO3[10], PD	Audio input0 Bit Clock, share with GPIO3[10]
I2S2_WS	**F4**	B,PD	8mA	VDD_IO_SYS	I,GPIO3[11], PD	Audio input0 Word Select For ADC, share with GPIO3[11]
I2S2_SDO	**E3**	B,PD	8mA	VDD_IO_SYS	I,GPIO3[12], PD	Audio output Serial Data Output to DAC, share with GPIO3[12]
I2S01_MCLK	**D2**	B,PD	8mA	VDD_IO_SYS	I,GPIO3[13], PD	Audio input0 Codec Master Clock, share with GPIO3[13]
I2S0_SCLK	**C3**	B,PD	8mA	VDD_IO_SYS	I,GPIO3[14], PD	Audio input0 Bit Clock, share with GPIO3[14]
I2S0_WS	**E2**	B,PD	8mA	VDD_IO_SYS	I,GPIO3[15], PD	Audio input0 Word Select For ADC, share with GPIO3[15]
I2S0_SDI	**C2**	B,PD	8mA	VDD_IO_SYS	I,GPIO3[16], PD	Audio input0 Serial Data Input From ADC, share with GPIO3[16]
EMAC_COL	**C19**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[0],PD	Collision detected, share with GPIO1[0]
EMAC_CRS	**D19**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[1],PD	Carrier sensor, share with GPIO1[1]
EMAC_RXD0	**C20**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[2],PD	Receive data bit0, share with GPIO1[2]
EMAC_RXD1	**D20**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[3],PD	Receive data bit1, share with GPIO1[3]
EMAC_RXD2	**C21**	B,PU	8mA	VDD_IO_SYS	I,GPIO1[4],PU	Receive data bit2, share with GPIO1[4]

EMAC_RXD3	**D21**	B,PU	8mA	VDD_IO_SYS	I,GPIO1[5],PU	Receive data bit3, share with GPIO1[5]
EMAC_RXER	**E20**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[6],PD	Receive error, share with GPIO1[6]
EMAC_RXDV	**H17**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[7],PD	Receive data valid, share with GPIO1[7]
EMAC_TXD0	**E21**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[8],PD	Transmit data bit0, share with GPIO1[8]
EMAC_TXD1	**H18**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[9],PD	Transmit data bit1, share with GPIO1[9]
EMAC_TXD2	**J17**	B,PU	8mA	VDD_IO_SYS	I,GPIO1[10],PU	Transmit data bit2, share with GPIO1[10]
EMAC_TXD3	**J18**	B,PU	8mA	VDD_IO_SYS	I,GPIO1[11],PU	Transmit data bit3, share with GPIO1[11]
EMAC_TXER	**K17**	B,PU	8mA	VDD_IO_SYS	I,GPIO1[12],PU	Transmit error, share with GPIO1[12]
EMAC_TXEN	**K18**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[13],PD	Transmit enable, share with GPIO1[13]
EMAC_MDIO	**L17**	B,PU	8mA	VDD_IO_SYS	I,GPIO1[14],PU	Management data I/O, share with GPIO1[14]
EMAC_MDC	**L18**	B,PU	8mA	VDD_IO_SYS	I,GPIO1[15],PU	Management Clock, share with GPIO1[15]
EMAC_RCK	**M17**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[16],PD	Receive Clock, share with GPIO1[16]
EMAC_TCK	**M18**	B,PD	8mA	VDD_IO_SYS	I,GPIO1[17],PD	Transmit Clock, share with GPIO1[17]
UHOST_RREFEXT	**M4**	AIO				USB HOST External Resistor For Current Reference (43.2Ohm, +- 1%)
UHOST_DP	**G1**	AIO				USB HOST D+ Port
UHOST_DM	**G2**	AIO				USB HOST D- Port
UOTG_RREFEXT	**L3**	AIO				USB OTG External Resistor For Current Reference (43.2Ohm, +- 1%)
UOTG_DP	**F1**	AIO				USB OTG D+ Port
UOTG_DM	**F2**	AIO				USB OTG D- Port
UOTG_ID	**G3**	AIO				USB Mini-Receptacle Identifier
UOTG_VBUS	**F3**	AIO				USB 5-V Power Supply Pin
ETH_TXP	**H2**	AIO				Transmit D+ Port, TXP
ETH_TXN	**H1**	AIO				Transmit D- Port, TXN
ETH_RXP	**J2**	AIO				Receive D+ Port, RXP
ETH_RXN	**J1**	AIO				Receive D- Port, RXN

ETH_RTX	**P3**	AIO				External 6K-Ohm 1% resistor to ground, RTX
SATA_SRESREF	**P6**	AO				SATA Port0 External Resistor
SATA_RX0_P	**N1**	AI				SATA Port0 Data Input+
SATA_RX0_M	**M2**	AI				SATA Port0 Data Input-
SATA_TX0_P	**L1**	AO				SATA Port0 Data Output+
SATA_TX0_M	**L2**	AO				SATA Port0 Data Output-
SATA_RX1_P	**P1**	AI				SATA Port1 Data Input+
SATA_RX1_M	**P2**	AI				SATA Port1 Data Input-
SATA_TX1_P	**T1**	AO				SATA Port1 Data Output+
SATA_TX1_M	**R2**	AO				SATA Port1 Data Output-
DDR_CSN	**AC3**	O		VDDQ_DDR	O,DDR_CSN	DDR SDRAM Chip Select
DDR_A[0]	**AB1**	O		VDDQ_DDR	O,DDR_A[0]	DDR SDRAM Memory Address 0
DDR_A[1]	**V23**	O		VDDQ_DDR	O,DDR_A[1]	DDR SDRAM Memory Address 1
DDR_A[2]	**W1**	O		VDDQ_DDR	O,DDR_A[2]	DDR SDRAM Memory Address 2
DDR_A[3]	**AB2**	O		VDDQ_DDR	O,DDR_A[3]	DDR SDRAM Memory Address 3
DDR_A[4]	**Y22**	O		VDDQ_DDR	O,DDR_A[4]	DDR SDRAM Memory Address 4
DDR_A[5]	**AA2**	O		VDDQ_DDR	O,DDR_A[5]	DDR SDRAM Memory Address 5
DDR_A[6]	**Y23**	O		VDDQ_DDR	O,DDR_A[6]	DDR SDRAM Memory Address 6
DDR_A[7]	**AA1**	O		VDDQ_DDR	O,DDR_A[7]	DDR SDRAM Memory Address 7
DDR_A[8]	**W22**	O		VDDQ_DDR	O,DDR_A[8]	DDR SDRAM Memory Address 8
DDR_A[9]	**Y1**	O		VDDQ_DDR	O,DDR_A[9]	DDR SDRAM Memory Address 9
DDR_A[10]	**AB23**	O		VDDQ_DDR	O,DDR_A[10]	DDR SDRAM Memory Address 10
DDR_A[11]	**W23**	O		VDDQ_DDR	O,DDR_A[11]	DDR SDRAM Memory Address 11
DDR_A[12]	**AA23**	O		VDDQ_DDR	O,DDR_A[12]	DDR SDRAM Memory Address 12
DDR_A[13]	**W2**	O		VDDQ_DDR	O,DDR_A[13]	DDR SDRAM Memory Address 13
DDR_A[14]	**V22**	O		VDDQ_DDR	O,DDR_A[14]	DDR SDRAM Memory Address 14
DDR_CLK_INV	**AB22**	O		VDDQ_DDR	O,DDR_CLK_INV	DDR SDRAM Clock Inverse, DDR_CLK_N

DDR_CLK	**AC22**	O		VDDQ_DDR	O,DDR_CLK	DDR SDRAM Clock, DDR_CLK_P
DDR_CKE	**AA21**	O		VDDQ_DDR	O,DDR_CKE	DDR SDRAM Clock Enable
DDR_CASN	**AA4**	O		VDDQ_DDR	O,DDR_CASN	DDR SDRAM Column Address Select
DDR_RASN	**AC5**	O		VDDQ_DDR	O,DDR_RASN	DDR SDRAM Row Address Select
DDR_WEN	**AC4**	O		VDDQ_DDR	O,DDR_WEN	DDR SDRAM Write Enable
DDR_DQM[0]	**AB18**	O		VDDQ_DDR	O,DDR_DQM[0]	DDR SDRAM Data Read/Write Mask 0 , DDR_DM[0]
DDR_DQM[1]	**AB8**	O		VDDQ_DDR	O,DDR_DQM[1]	DDR SDRAM Data Read/Write Mask 1 , DDR_DM[1]
DDR_DQM[2]	**Y16**	O		VDDQ_DDR	O,DDR_DQM[2]	DDR SDRAM Data Read/Write Mask 2 ,DDR_DM[2]
DDR_DQM[3]	**Y10**	O		VDDQ_DDR	O,DDR_DQM[3]	DDR SDRAM Data Read/Write Mask 3 , DDR_DM[3]
DDR_BA[0]	**AC2**	O		VDDQ_DDR	O,DDR_BA[0]	DDR SDRAM Bank Access 0
DDR_BA[1]	**AA22**	O		VDDQ_DDR	O,DDR_BA[1]	DDR SDRAM Bank Access 1
DDR_BA[2]	**AB3**	O		VDDQ_DDR	O,DDR_BA[2]	DDR SDRAM Bank Access 2
DDR_DQ[0]	**AC7**	B		VDDQ_DDR	B,DDR_DQ[0]	DDR SDRAM Data 0
DDR_DQ[1]	**AB5**	B		VDDQ_DDR	B,DDR_DQ[1]	DDR SDRAM Data 1
DDR_DQ[2]	**AC8**	B		VDDQ_DDR	B,DDR_DQ[2]	DDR SDRAM Data 2
DDR_DQ[3]	**AB6**	B		VDDQ_DDR	B,DDR_DQ[3]	DDR SDRAM Data 3
DDR_DQ[4]	**AC19**	B		VDDQ_DDR	B,DDR_DQ[4]	DDR SDRAM Data 4
DDR_DQ[5]	**AB21**	B		VDDQ_DDR	B,DDR_DQ[5]	DDR SDRAM Data 5
DDR_DQ[6]	**AC20**	B		VDDQ_DDR	B,DDR_DQ[6]	DDR SDRAM Data 6
DDR_DQ[7]	**AB20**	B		VDDQ_DDR	B,DDR_DQ[7]	DDR SDRAM Data 7
DDR_DQ[8]	**AC16**	B		VDDQ_DDR	B,DDR_DQ[8]	DDR SDRAM Data 8
DDR_DQ[9]	**AC11**	B		VDDQ_DDR	B,DDR_DQ[	DDR SDRAM Data 9

					9]	
DDR_DQ[10]	**AC17**	B		VDDQ_DDR	B,DDR_DQ[10]	DDR SDRAM Data 10
DDR_DQ[11]	**AC10**	B		VDDQ_DDR	B,DDR_DQ[11]	DDR SDRAM Data 11
DDR_DQ[12]	**AB15**	B		VDDQ_DDR	B,DDR_DQ[12]	DDR SDRAM Data 12
DDR_DQ[13]	**AB9**	B		VDDQ_DDR	B,DDR_DQ[13]	DDR SDRAM Data 13
DDR_DQ[14]	**AB17**	B		VDDQ_DDR	B,DDR_DQ[14]	DDR SDRAM Data 14
DDR_DQ[15]	**AB11**	B		VDDQ_DDR	B,DDR_DQ[15]	DDR SDRAM Data 15
DDR_DQ[16]	**AA9**	B		VDDQ_DDR	B,DDR_DQ[16]	DDR SDRAM Data 16
DDR_DQ[17]	**AA17**	B		VDDQ_DDR	B,DDR_DQ[17]	DDR SDRAM Data 17
DDR_DQ[18]	**Y9**	B		VDDQ_DDR	B,DDR_DQ[18]	DDR SDRAM Data 18
DDR_DQ[19]	**AA18**	B		VDDQ_DDR	B,DDR_DQ[19]	DDR SDRAM Data 19
DDR_DQ[20]	**AA8**	B		VDDQ_DDR	B,DDR_DQ[20]	DDR SDRAM Data 20
DDR_DQ[21]	**Y18**	B		VDDQ_DDR	B,DDR_DQ[21]	DDR SDRAM Data 21
DDR_DQ[22]	**Y8**	B		VDDQ_DDR	B,DDR_DQ[22]	DDR SDRAM Data 22
DDR_DQ[23]	**Y17**	B		VDDQ_DDR	B,DDR_DQ[23]	DDR SDRAM Data 23
DDR_DQ[24]	**AA15**	B		VDDQ_DDR	B,DDR_DQ[24]	DDR SDRAM Data 24
DDR_DQ[25]	**AA12**	B		VDDQ_DDR	B,DDR_DQ[25]	DDR SDRAM Data 25
DDR_DQ[26]	**AA10**	B		VDDQ_DDR	B,DDR_DQ[26]	DDR SDRAM Data 26
DDR_DQ[27]	**AA16**	B		VDDQ_DDR	B,DDR_DQ[27]	DDR SDRAM Data 27
DDR_DQ[28]	**AA11**	B		VDDQ_DDR	B,DDR_DQ[28]	DDR SDRAM Data 28
DDR_DQ[29]	**Y11**	B		VDDQ_DDR	B,DDR_DQ[29]	DDR SDRAM Data 29
DDR_DQ[30]	**Y15**	B		VDDQ_DDR	B,DDR_DQ[	DDR SDRAM Data 30

					30]	
DDR_DQ[31]	**Y14**	B		VDDQ_DDR	B,DDR_DQ[31]	DDR SDRAM Data 31
DDR_DQS[0]	**AB12**	B		VDDQ_DDR	B,DDR_DQS[0]	DDR SDRAM Data Strobe byte 0 , DDR_DQS0_P
DDR_DQS[1]	**AC14**	B		VDDQ_DDR	B,DDR_DQS[1]	DDR SDRAM Data Strobe byte 1 , DDR_DQS1_P
DDR_DQS[2]	**Y12**	B		VDDQ_DDR	B,DDR_DQS[2]	DDR SDRAM Data Strobe byte 2 , DDR_DQS2_P
DDR_DQS[3]	**Y13**	B		VDDQ_DDR	B,DDR_DQS[3]	DDR SDRAM Data Strobe byte 3 , DDR_DQS3_P
DDR_DQS_INV[0]	**AC13**	B		VDDQ_DDR	B,DDR_DQS_INV[0]	DDR SDRAM Data Strobe Inverse byte 0 , DDR_DQS0_N
DDR_DQS_INV[1]	**AB14**	B		VDDQ_DDR	B,DDR_DQS_INV[1]	DDR SDRAM Data Strobe Inverse byte 1 , DDR_DQS1_N
DDR_DQS_INV[2]	**AA13**	B		VDDQ_DDR	B,DDR_DQS_INV[2]	DDR SDRAM Data Strobe Inverse byte 2 , DDR_DQS2_N
DDR_DQS_INV[3]	**AA14**	B		VDDQ_DDR	B,DDR_DQS_INV[3]	DDR SDRAM Data Strobe Inverse byte 3 , DDR_DQS3_N
DDR_RSTN	**Y2**	O		VDDQ_DDR	O,DDR_RSTN	DDR SDRAM Reset Signal, only for DDR3
DDR_ODT	**AB4**	O		VDDQ_DDR	O,DDR_ODT	DDR SDRAM On Die Termination, only for DDR2
DDR_ZQ	**Y19**	B		VDDQ_DDR	B,DDR_ZQ	DDR SDRAM ZQ
DDR_DLL_DTO[0]	**V17**	O		VDDQ_DDR	O,DDR_DLL_DTO[0]	DDR DLL Digital Test Output 0, for Test
DDR_DLL_DTO[1]	**V18**	O		VDDQ_DDR	O,DDR_DLL_DTO[1]	DDR DLL Digital Test Output 1, for Test
DDR_DLL_ATO	**AA19**	B		VDDQ_DDR	B,DDR_DLL_ATO	DDR DLL Analog Test Output, for Test
VGA0_HSYNC	**L20**	B,PD	8mA		I,GPIO1[18], PD	VGA0 HSYNC, share with GPIO1[18]
VGA0_VSYNC	**M21**	B,PD	8mA		I,GPIO1[19], PD	VGA0 VSYNC, share with GPIO1[19]
VDAC0_OUTP0	**R23**	AO				VDAC0 OUT0 +
VDAC0_OUTP1	**P23**	AO				VDAC0 OUT1 +
VDAC0_OUTP2	**P22**	AO				VDAC0 OUT2 +
VDAC0_REXT	**T20**	AIO				VDAC0 Reference External

VDAC0_VDREF	**R22**	AIO				VDAC0 VD Reference
VGA1_HSYNC	**M20**	B,PD	8mA		I,GPIO1[20], PD	VGA1 HSYNC, share with GPIO1[20]
VGA1_VSYNC	**L21**	B,PD	8mA		I,GPIO1[21], PD	VGA1 VSYNC, share with GPIO1[21]
VDAC1_OUTP0	**T23**	AO				VDAC1 OUT0 +
VDAC1_OUTP1	**U23**	AO				VDAC1 OUT1 +
VDAC1_OUTP2	**U22**	AO				VDAC1 OUT2 +
VDAC1_REXT	**T21**	AIO				VDAC1 Reference External
VDAC1_VDREF	**T22**	AIO				VDAC0 VD Reference
HDMI_TX2P	**B18**	AO				Channel 2 TX+
HDMI_TX2N	**A18**	AO				Channel 2 TX-
HDMI_TX1P	**B19**	AO				Channel 1 TX+
HDMI_TX1N	**A19**	AO				Channel 1 TX-
HDMI_TX0P	**B20**	AO				Channel 0 TX+
HDMI_TX0N	**A20**	AO				Channel 0 TX-
HDMI_TXCP	**B21**	AO				TX Clock+
HDMI_TXCN	**A21**	AO				TX Clock-
HDMI_RBIAS	**A15**	AI				12KOhm resistor to Ground，+/-1%
HDMI_CEC	**C15**	B,PD	8mA	VDD_IO_HDMI	I,GPIO1[22], PD	Custom Electronics Control Wire, share with GPIO1[22]
HDMI_DSCL	**C16**	B,PU	8mA	VDD_IO_HDMI	I,GPIO1[23], PU	I2C Master Clock, share with GPIO1[23]
HDMI_DSDA	**C17**	B,PU	8mA	VDD_IO_HDMI	I,GPIO1[24], PU	I2C Master Data, share with GPIO1[24]
HDMI_HPD	**C18**	B,PD	8mA	VDD_IO_HDMI	I,GPIO1[25], PD	Hot Plug Detect, share with GPIO1[25]
VDDA_PLL0	**K23**	PWR		1.0v		PLL0 Analog Power,1.0V
VDDA_PLL1	**K22**	PWR		1.0v		PLL1 Analog Power,1.0V
VDDA_PLL2	**L23**	PWR		1.0v		PLL2 Analog Power,1.0V
VDDA_PLL3	**L22**	PWR		1.0v		PLL3 Analog Power,1.0V
VDDA_PLL4	**N21**	PWR		1.0v		PLL4 Analog Power,1.0V
VSSA_PLL0	**K21**	GND		0v		PLL0 Analog Ground
VSSA_PLL1	**M22**	GND		0v		PLL1 Analog Ground

VSSA_PLL2	**M23**	GND		0v		PLL2 Analog Ground
VSSA_PLL3	**N23**	GND		0v		PLL3 Analog Ground
VSSA_PLL4	**N22**	GND		0v		PLL4 Analog Ground
UHOST_VDDA33	**K4**	PWR		3.3v		USB HOST PHY Analog Power 3.3v
UHOST_VSSA33	**M6**	GND		0v		USB HOST PHY Analog Ground , UHOST_VSSA
UHOST_VSSAC	**N3**	GND		0v		USB HOST PHY PLL Analog Ground
UOTG_VDDA33	**L6**	PWR		3.3v		USB OTG PHY Analog Power 3.3v
UOTG_VSSA33	**K3**	GND		0v		USB OTG PHY Analog Ground 3.3v , UOTG_VSSA33
UOTG_VSSAC	**M3**	GND		0v		USB OTG PHY PLL Analog Ground
VDD33_EPHY	**K1, K2**	PWR		3.3v		ETHERNET PHY Analog Power supply:3.3v
VSS_EPHY	**N4, P4**	GND		0v		ETHERNET PHY Analog Ground
SPHY_VP25	**T3，T4，R3，R4**	PWR		2.5v		SATA PHY Analog Power high voltage supply:2.5v
VDAC0_PVDD1	**R20**	PWR		3.3v		VDAC0 Analog Power,3.3v
VDAC0_PVDD2	**R21**	PWR		3.3v		VDAC0 Analog Power,3.3v
VDAC0_PGND1	**P20,P21**	GND		0v		VDAC0 Analog Ground
VDAC1_PVDD1	**U20,V20,V21**	PWR		3.3v		VDAC1 Analog Power,3.3v
VDAC1_PVDD2	**U21**	PWR		3.3v		VDAC1 Analog Power,3.3v
VDAC1_PGND1	**W20,W21**	GND		0v		VDAC1 Analog Ground
AVDD33_ESD	**A17,B17**	PWR		3.3v		HDMI ESD Analog Power 3.3v
AVSS33_ESD	**A16,B16**	GND		0v		HDMI ESD Analog Ground
AVDD33_HDMI	**A14**	PWR		3.3v		HDMI Analog Power 3.3v
AVSS33_HDMI	**B15**	GND		0v		HDMI Analog Ground
HDMI_VSS3IO	**C14,D14**	GND		0v		DVSS,ESD Ground

VDD_CORE	**N10-N15, N17, P10-P15, P17-P18, R10-R15, R17-R18, T17-T18, U10-U18**	PWR		1.0v		Core power,1.0v
VDD_IO_SYS	**A22, J6-J7, H7, K6, H22-23, K20,**	PWR		3.3v		System Digital I/O power,3.3v
VDD_IO_DCVI	**B8-B9, C8-C9**	PWR		1.8v,3.3v		DCVI Digital I/O power
VDD_IO_HDMI	**D15**	PWR		5.0v		HDMI Digital I/O power
VDD_IO_LCD	**D16,D17,F7,F8, G7,G8,F14,G14**	PWR		2.8v,3.3v		LCD Digital I/O power
VDD_IO_DDR	**U1-U4, U6-U7, V1-V4, V6-V8, W3-W4, Y3-Y5, AA3, AA5**	PWR		1.5v		DRAM Power,1.5v
DDR_PLL_VDD	**V11-V13,**	PWR		2.5v		DDR PLL Power,2.5v
DDR_PLL_VSS	**V14-V16**	GND		0v		DDR PLL Ground
VREF_DDR	**Y21**	PWR		1/2 VDDQ_DDR		DRAM REF Power , DDR_VREF
VSS	**A1,AC1,A23,AC23,B14,D18,G22,K7,K9-15,L7,L4,L9-L15,M1,M7, M9-15,N6-N7,N2,N9,P7,P9,R1, R6-7,R9,T2,T6-7,U8-9,V9-10,Y6-7,AA6-7,AB7,AC6,AC9,AB10,AC12,AB13,AC15,AB16,AC18,AB19,Y20,AA20,AC21,N18,N20,G22,D18,B14**	GND		0v		System Digital I/O ground