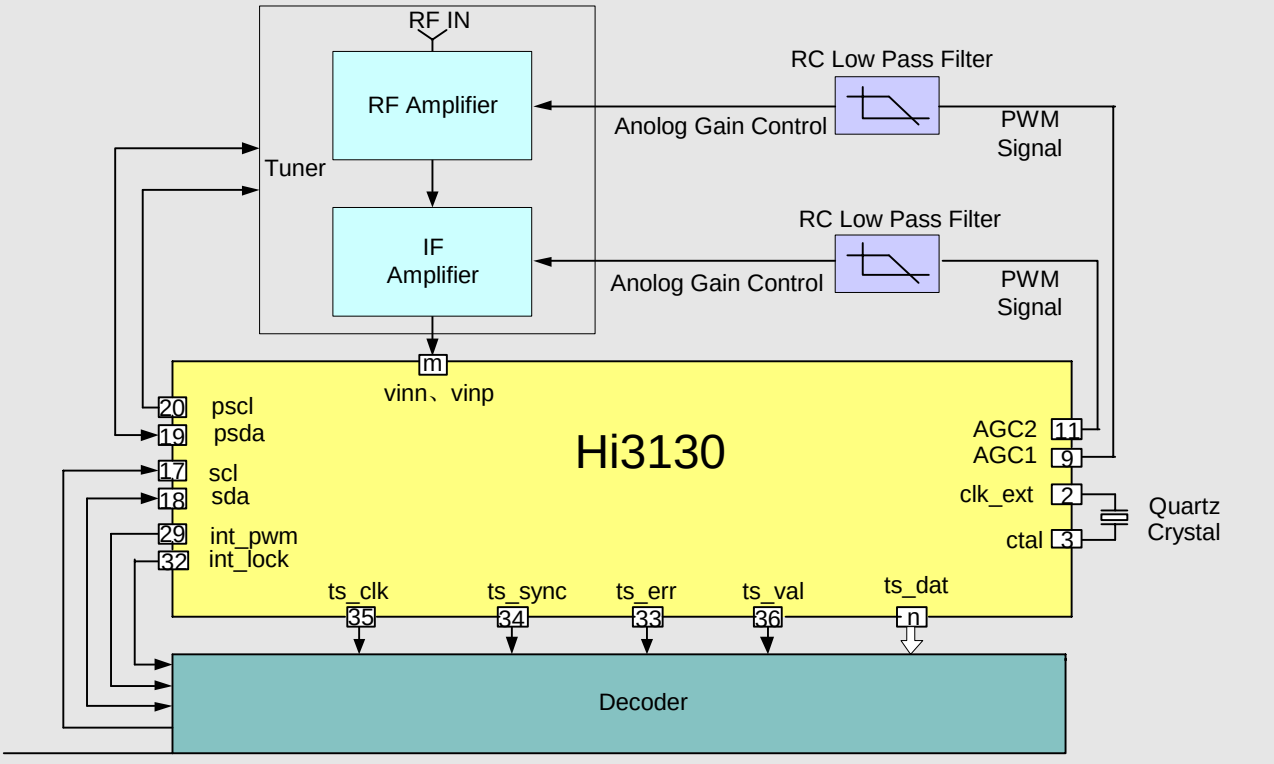
Hi3130 Cable Digital TV Channel Receiver

Features

- Compliant with the DVB-C standard
- 16/32/64/128/256-QAM demodulation
- An integrated high performance 12-bit IF ADC, intended for all Direct IF and Low IF solutions
- Adaptive digital down sampling and anti-aliasing filter, with variable symbol rates from 0.87 Mbaud to 9 Mbaud
- Adaptive digital carrier recovery, supporting up to 800 kHz frequency deviation
- Adaptive digital timing recovery, supporting up to 500 ppm big symbol rate deviation
- Automatic bandwidth select matched filtering, with the raised cosine roll-off factor from 0.12 to 0.2
- Adaptive blind equalization and decision feedback equalization, effective in correcting various micro reflections and typical distortions
- Integrated forward error correction decoding, compliant with the ITU J83-A/C stream specification
- Dual AGCs
- Internal registers controlled and monitored through the two-wire bus
- Real-time signal quality monitoring
- Interrupt generation
- Chip status indication
- Programmable output clock
- Compliant with the common DVB interface standard
- Serial or parallel TS output
- Automatically detecting and correcting for spectrum inversion
- Channel blind scan
- Integrated PLL, externally connected to the LF crystal or sharing the same clock source with the decoder and the demodulator
- Integrated crystal oscillator circuit. The system clock can be generated on chip through the external crystal.
- Low power consumption (in case of 6.9 Msymb/s, the typical power consumption is 300 mW)
- Support for software control on the power saving mode
- LQFP64 package
- 1.8 V/3.3 V power voltage

Applications and Typical Application Diagram

- Cable tuners
- Cable set-top boxes (STBs) and integrated digital TV sets
- Cable modems and digital TV cards



Note: n ranges from 48 to 45 and from 40 to 37; m ranges from 57 to 58.

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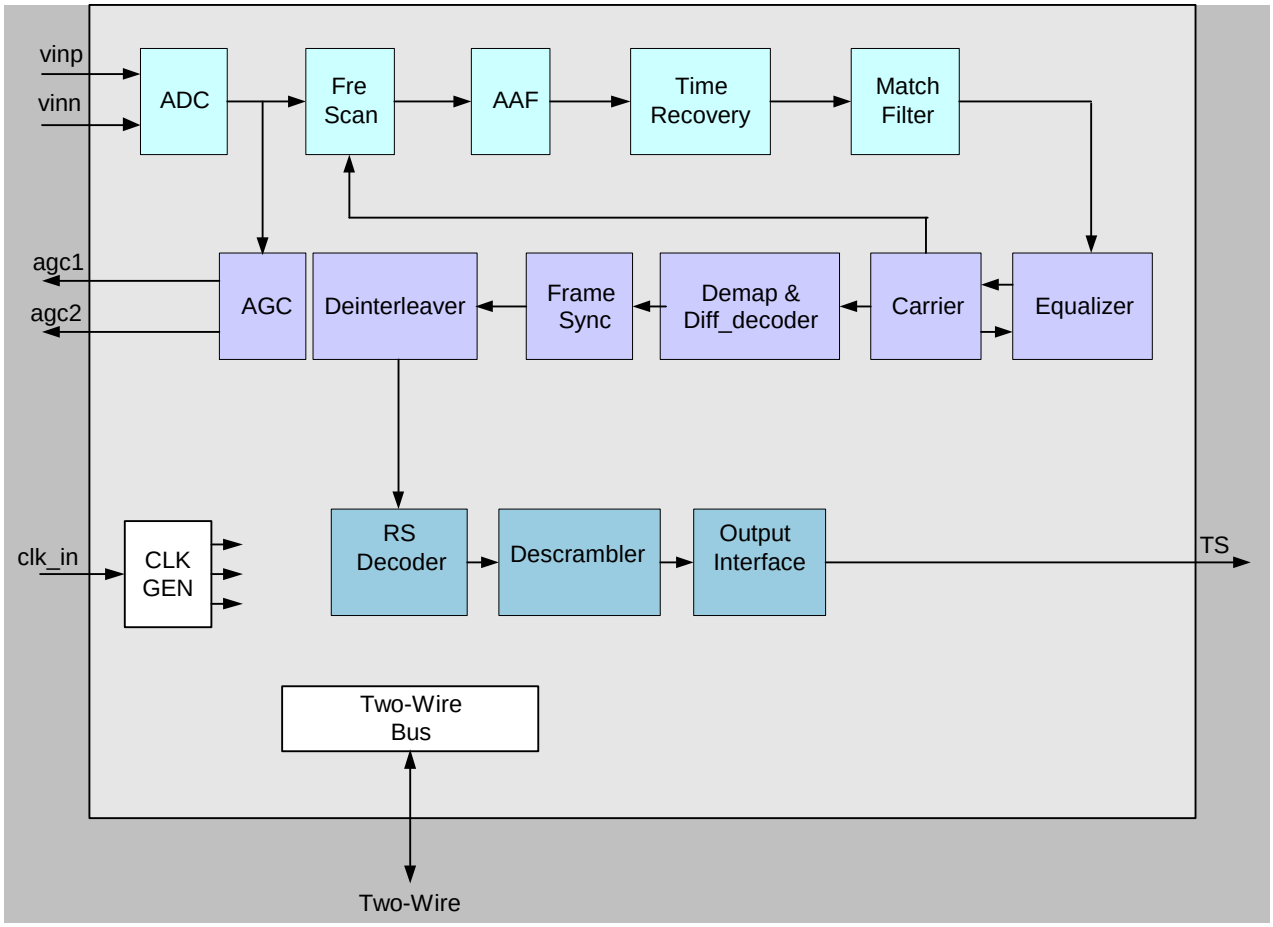
Functional Block Diagram



The Hi3130 is a single-chip cable digital TV channel receiving chip. It is compliant with DVB-C (ETS 300 429), ITU J83-A and ITU J83-C specifications. The Hi3130 provides powerful 16/32/64/128/256-QAM demodulation and forward error correction capabilities. It is intended for the complete processing toward cable digital signals, from IF sampling to MPEG-TS output. Thus it offers solutions for the reception of TV signals and other data signals over coaxial cables.

The Hi3130 integrates a high performance analog digital converter (ADC) with 10-bit resolution and up to 40 Msps sampling rate. This converter is able to handle IF sampling of up to 256-QAM signals. Fully digital processing comes after IF sampling. According to complex channel details, the Hi3130 provides all necessary functions, including demodulation, micro reflection cancellation and RS forward error correction. It monitors the chip status and the signal quality to work together with the decoder chip. In addition, two AGCs and a two-wire bus are used to control the tuner and ease the design of application boards.

The MPEG-TS output by the Hi3130 is compatible with the DVB standard interface and can seamlessly connect to the MPEG decoder.

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