Hi3136 Satellite Digital TV Channel Receiver Chipset

Key Specifications

Demodulation

- DVB-S2, DVB-S, and DirecTV (ITU-R BO.1516-System B) standards, automatic standard recognition
- QPSK, 8PSK, 16APSK, and 32APSK for DVB-S2
- 11 code rates for DVB-S2
- Short and long frames for DVB-S2
- CCM, VCM, and ACM modes for DVB-S2
- TSs and GSs for DVB-S2, data services support

Features

- Rapid and reliable blind scanning at full frequency bands to automatically obtain system information such as the carrier frequency, symbol rate, and code rate
- Superior phase noise suppression
- Superior anti-multipath for reducing reflections from high buildings and impedance mismatch
- Superior anti-interference for improving environment adaptation
- Rapid channel synchronization for reducing channel switching time
- Wide carrier and symbol rate acquisition ranges for improving applicability
- Adaptive spectrum inversion recognition
- A maximum bit rate of 187.5 Mbit/s
- A minimum symbol rate of 1 Msps and the following maximum symbol rates:
  - 60 Msps in QPSK or 8PSK mode
  - 47 Msps in 16APSK mode
  - 37.5 Msps in 32APSK mode

System

- Integrated 125 MHz and 10-bit ADC with dual channels for supporting highly accurate sampling
- Integrated PLL, external passive crystal oscillator, 10−30 MHz (24 MHz typically)
- Real-time monitoring of the signal strength, signal-to-noise ratio, and bit error rate
- Simple external circuits, 2-layer PCB routing, low BOM costs

Interfaces

- I^2C bus protocol support for flexibly controlling chipsets
- Tuner I^2C bus trunk
- DiSEqC V2.*x* and FSK protocol support for controlling satellite equipment
- TS outputs in configurable serial or parallel mode to work with decoding chipsets
- Configurable TS output pin for facilitating PCB routing

Process

- 1.2 V core power supply, 3.3 V I/O power supply, and maximum power consumption of 540 mW
- MQFN48, body size of 6 mm x 6 mm (0.24 in. x 0.24 in.), RoHS compliance

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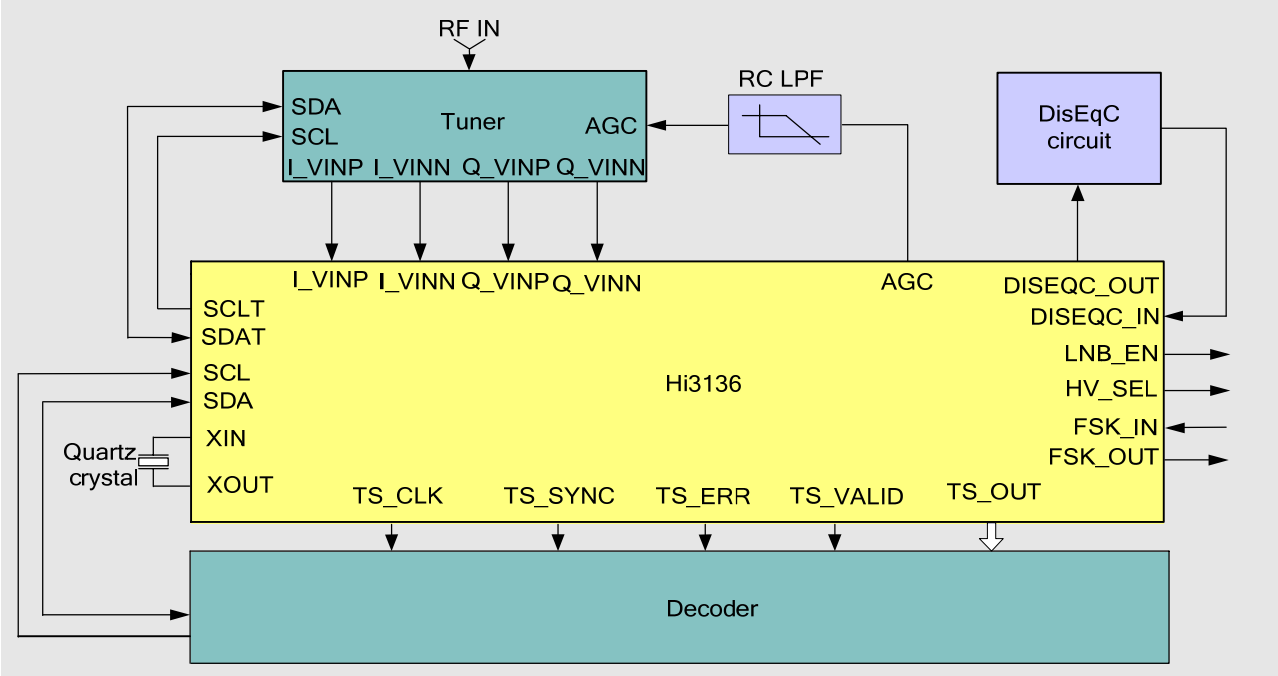
Application Fields and Typical Application Diagram

- Satellite tuner
- Satellite STB and integrated digital TV
- Satellite modem and digital TV card



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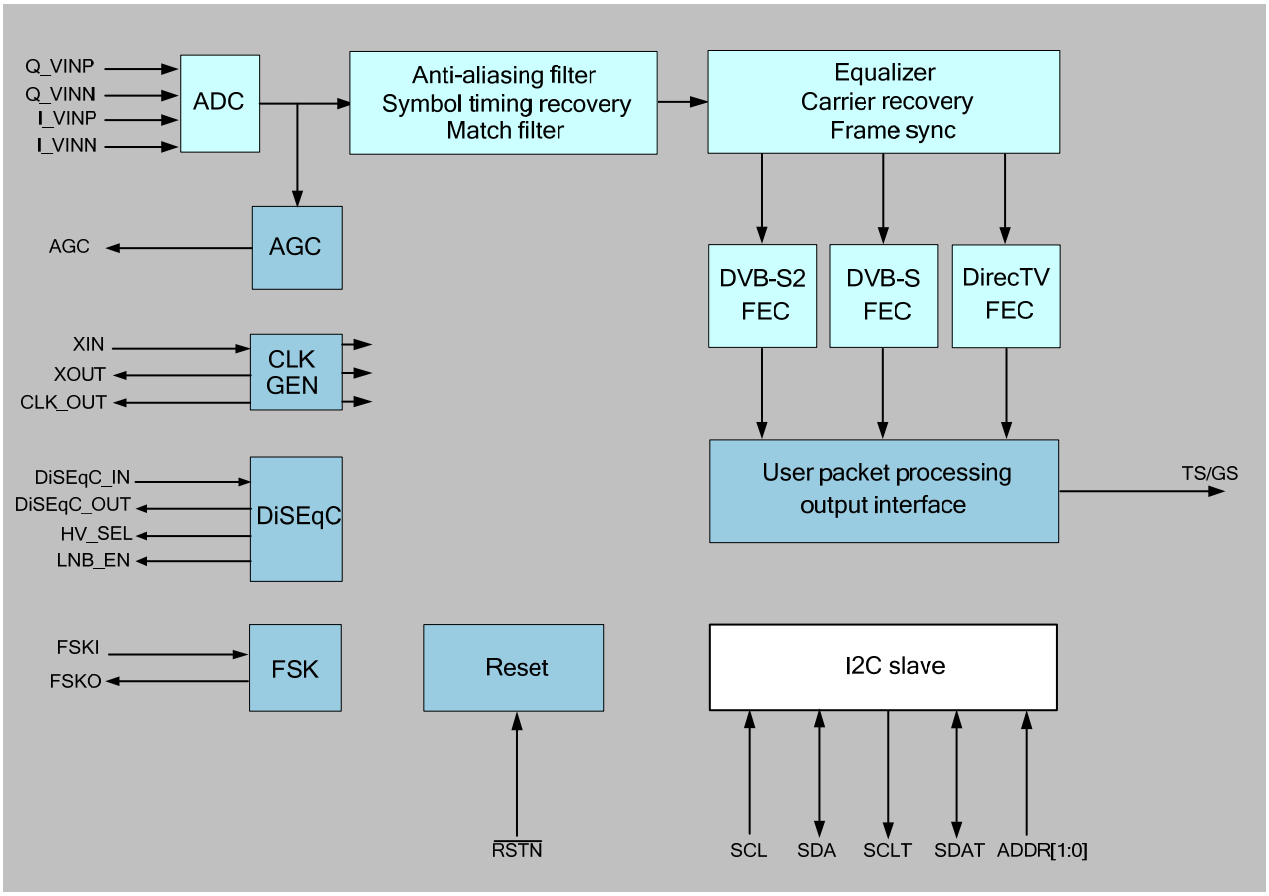
Functional Block Diagram



Hi3136 V100 is a satellite digital TV channel receiver chipset that supports DVB-S (ETS 300 421), DVB-S2 (ETS 302 307), and DirecTV (ITU-R BO.1294-System B) standards. The chipset uses all-digital processing technologies from baseband sampling on satellite digital signals to MPEG TS output. With the following features in the DVB-S2 standard, Hi3136 V100 provides the most comprehensive functions in the industry and offers high applicability:

- Supports QPSK, 8PSK, 16APSK, and 32APSK modes.
- Supports code rates from 1/4 to 9/10.
- Supports long and short frames.
- Supports CCM, VCM, and ACM modes.
- Processes TSs and GSs.

Hi3136 V100 supports the minimum symbol rate of 1 Msps and the maximum symbol rate of 60 Msps in QPSK or 8PSK mode, 47 Msps in 16APSK mode, or 37.5 Msps in 32APSK mode. These features enable Hi3136 V100 to support ultra-low-speed to ultra-high-speed services.

Hi3136 V100 provides rapid and reliable blind scanning to search programs at full frequency bands and to obtain information such as the frequency, symbol rate, and code rate. Hi3136 V100 also supports phase noise suppression, anti-multipath, and anti-interference. It has a wide carrier frequency acquisition range and is able to work in various environments.

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Hi3136 V100 interacts with the CPU over the I^2C interface to monitor the signal strength, signal quality, and bit error rate in real time, which helps customers search satellite signals by adjusting the antenna. Hi3136 V100 supports the DiSEqC V2.*x* protocol and FSK protocol. This facilitates interconnection between Hi3136 V100 and satellite equipment. Hi3136 V100 provides serial and parallel TS output interfaces and a configurable signal line sequence, facilitating PCB routing. In addition, Hi3136 V100 has simple external circuits and supports 2-layer PCB routing, which reduces BOM costs.

Acronyms and Abbreviations

ACM	adaptive coding and modulation
ADC	analog-to-digital converter
APSK	absolute phase shift keying
BOM	bill of material
CCM	constant coding and modulation
DiSEqC	digital satellite equipment control
DVB-S	digital video broadcasting-satellite
FSK	frequency shift keying
GS	generic stream
I^2C	inter-integrated circuit
I/O	input/output
ITU	International Telecommunication Union
MQFN	mapped quad flat non-leaded
PCB	printed circuit board
PLL	phase locked loop
PSK	phase shift keying
QPSK	quaternary phase shift keying
RoHS	restriction of the use of certain hazardous substances
STB	set-top box
TS	transport stream
TV	television
VCM	variable coding and modulation

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