Hi3137 V100 Terrestrial Digital TV Channel Receiver Chip

Key Specifications

Demodulation

- DVB-T2 and DVB-T standards, automatic standard recognition
- Standard DVB-T2 V1.3.1 and DVB-T V1.5.1
- DVB-T2 Base and Lite modes
- 5 MHz, 6 MHz, 7 MHz, 8 MHz, and 1.7 MHz input bandwidth
- Single PLP and Multi PLP services and SISO and MISO transmission support for DVB-T2
- Automatic common PLP and data PLP combination by DVB-T2
- TSs and common streams (GCS/GFPS/GSE) support for DVB-T2, adapting to data services
- All parameter mode support for DVB-T, including layered transmission and non-layered transmission

Features

- Compliant with various European test standards, including DTG7.0, NorDig-Unified Test Specification V2.2.1, and Digital Europe Ebook
- Low IF and high IF (36 MHz) signal inputs
- Rapid signal picking up capability (less than 250 ms for DVB-T signals and less than 500 ms for DVB-T2 signals), reducing the wait time for switching the channel
- Superior Gaussian, multipath, and mobile reception performance, adapting to terrestrial signal reception in various scenarios
- Superior anti-interference (from the same frequency) performance
- Adaptive spectrum reverse recognition
- Frequency error detecting range broader than [–700 kHz, +700 kHz]

System

- Integrated 12-bit high-performance ADC for supporting highly accurate sampling
- Integrated PLL, external passive crystal oscillator, 10−30 MHz (24 MHz typically), ±150 ppm frequency error
- Real-time monitoring of the signal strength, signal quality, and bit error rate

Interfaces

- I^2C bus protocol (slave) support for flexibly controlling the chip
- TS outputs in configurable serial or parallel mode to work with the decoding chipset
- Configurable TS output pin for facilitating PCB routing
- Simple external circuits, 2-layer PCB routing, low BOM costs

Process

- 1.1 V core power supply, 3.3 V I/O power supply
- Low-power design, less than 500 mW power consumption with full loads, 350mW with typical loads
- MQFN48, body size of 6 mm x 6 mm (0.24 in. x 0.24 in.)

Application Fields and Typical Application Diagram

- Terrestrial digital signal tuner
- Terrestrial digital STB and integrated digital TV
- Modem and digital TV card

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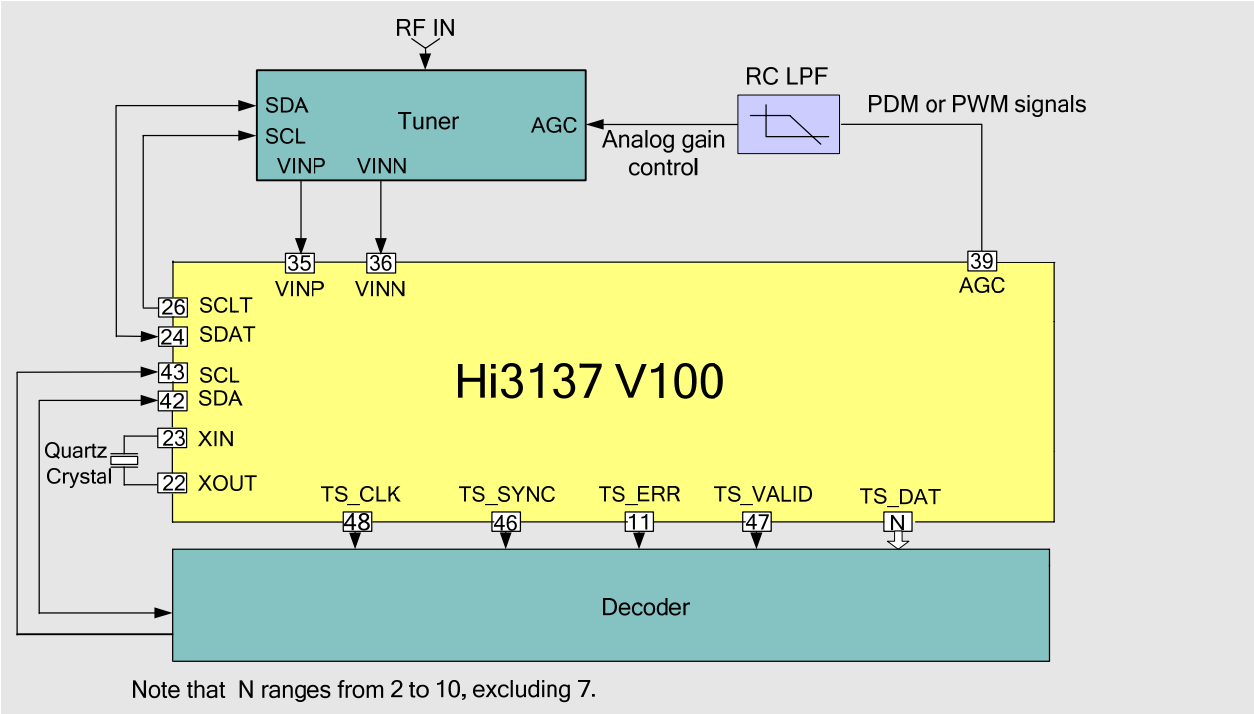

Note that N ranges from 2 to 10, excluding 7.

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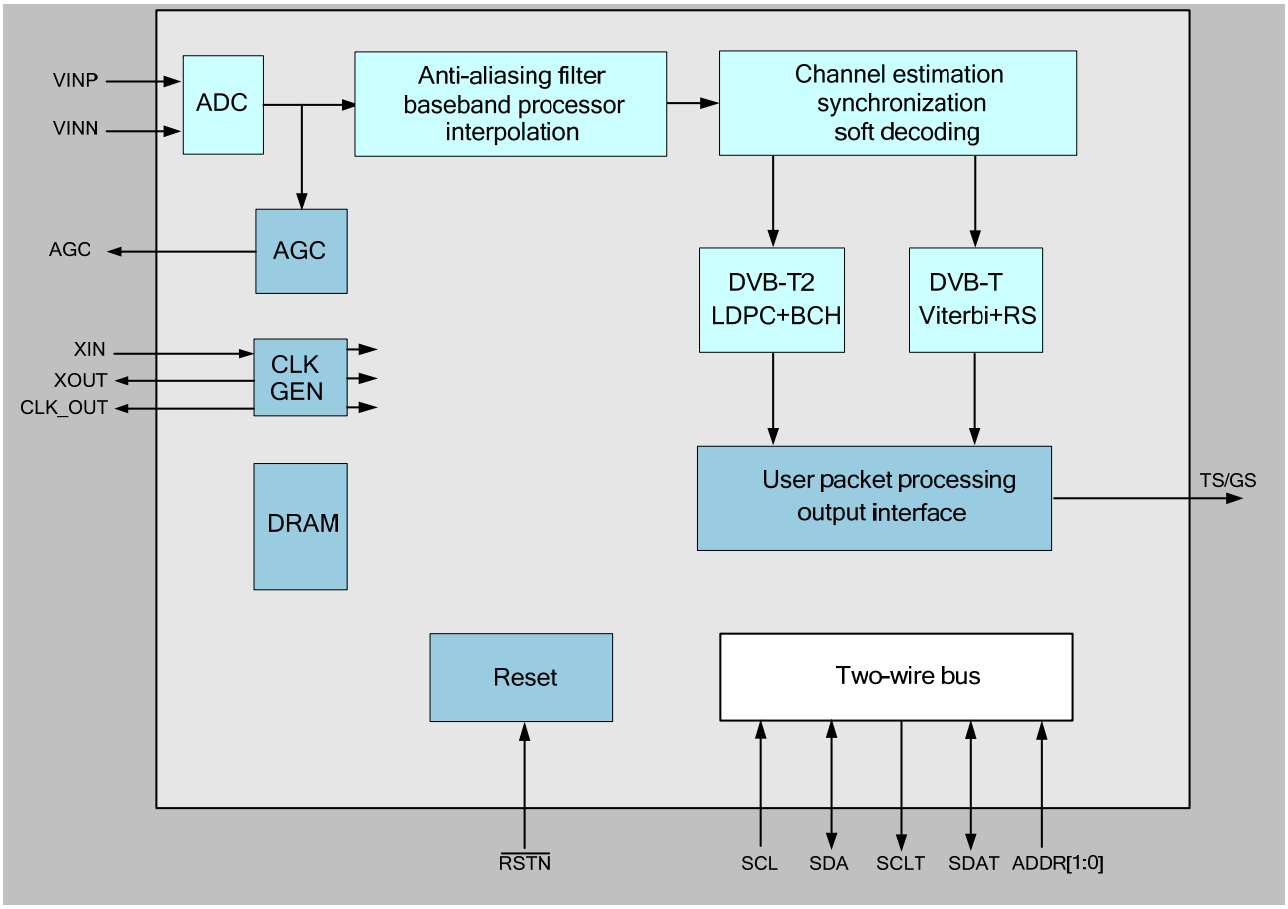
Functional Block Diagram



Hi3137 V100 is a terrestrial digital TV channel receiver chip that supports DVB-T and DVB-T2 modes. Complying with the DVB-T2 (ETS 302 755) and DVB-T (ETS 300 744) standards, it provides the high-performance multi-carrier demodulation capability and forward error correction function to implement full processing from baseband sampling on terrestrial digital signals to MPEG TS output.

Hi3137 V100 interacts with the CPU over the I^2C interface to monitor the signal strength, signal quality, and bit error rate in real time, which helps users search for signals by adjusting the antenna. Hi3137 V100 provides serial and parallel TS output interfaces. The signal line sequence can be configured, facilitating PCB routing.

Hi3137 V100 uses the low-power design. When the signal quality is above the critical point, the power consumption is less than 350 mW. When the signal quality is at the critical point, the power consumption is less than 500 mW. The chip uses the MQFN48 package (with EPAD) with the body size of 6 mm x 6 mm (0.24 in. x 0.24 in.). In addition, Hi3137 V100 has simple external circuits and supports 2-layer PCB routing, which reduces the BOM cost.

The SDK contains the debugging tools for the PC end. You can customize various debugging functions during development.

Acronyms and Abbreviations

ADC	analog-to-digital converter

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BOM	bill of material
DVB-T	digital video broadcasting-terrestrial
I^2C	inter-integrated circuit
IF	intermediate frequency
I/O	input/output
PCB	printed circuit board
PLL	phase locked loop
SDK	software development kit
STB	set-top box
TS	transport stream
TV	television

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