



Hi3796M V200 Brief Data Sheet

Key Specifications

High-Performance CPU

- 64-bit quad-core high-performance ARM Cortex A53
- Integrated multimedia acceleration engine NEON
- Hardware Java acceleration
- Integrated hardware floating-point coprocessor
- Integrated L1 and L2 Cache

3D GPU

- Integrated high-performance multi-core GPU Mali 450
- OpenGL ES 2.0/1.1 and OpenVG 1.1

Memory Control Interfaces

- DDR3/DDR3L/DDR4 interface, supporting maximum 32-bit data width
- eMMC 5.0 flash interface
- SPI NOR flash interface
- SPI NAND flash interface
- Asynchronous/Synchronous NAND flash interface
 - SLC/MLC flash memory
 - Maximum 64-bit ECC

Video Decoding (HiVXE 2.0 Processing Engine)

- AVS2 Main-10bit Profile, Level 8.2.60, supporting maximum 4K x 2K@60 fps 10-bit decoding
- H.265/HEVC Main/Main 10 Profile@Level 5.1 high-tier, supporting maximum 4K x 2K@60 fps 10-bit decoding
- Maximum 4K x 2K@60 fps 10-bit decoding for VP9
- H.264/AVC BP/MP/HP@Level 5.1; H.264/AVC MVC, supporting maximum 4K x 2K@30 fps decoding
- Maximum 1080p@60 fps decoding for Real 8/9/10
- Maximum 1080p@60 fps decoding for MPEG-1
- MPEG-2 SP@ML, MP@HL, supporting maximum 1080p@60 fps decoding
- MPEG-4 SP@Levels 0–3, ASP@Levels 0–5, supporting GMC, short header format, and maximum 1080p@60 fps decoding
- AVS Baseline Profile@Level 6.0, AVS-P16 (AVS+), supporting maximum 1080p@60 fps decoding
- VC-1 SP@ML, MP@HL, AP@Levels 0–3, supporting maximum 1080p@60 fps decoding

Image Decoding

- JPEG decoding, supporting maximum 64 megapixels
- PNG decoding, supporting maximum 64 megapixels

Video and Image Encoding

- H.265 MP@Level 5 main tier and H.264 BP/MP/HP@Level 4.2 video encoding, supporting maximum 1-channel 1080p@30 fps encoding
- VBR or CBR mode for video encoding
- Low-delay encoding
- Encoding of multiple ROIs

Audio Encoding and Decoding

- Integrated audio DSP
- MPEG L1/L2
- Dolby Digital/Dolby Digital Plus decoder-converter
- Dolby TrueHD decoding
- Dolby Digital/DTS transparent transmission
- Dolby MS12 with DAP and Dolby Atmos pass-through
- DTS HD/DTS M6 decoding

- AAC-LC and HE-AAC V1/V2 decoding
- APE, FLAC, Ogg, AMR-NB, and AMR-WB decoding
- G.711 (u/a) audio decoding
- G.711 (u/a), AMR-NB, AMR-WB, and AAC-LC audio encoding
- HE-AAC transcoding DD (AC3)

Channel Decoding and TS De-multiplexing

- One embedded QAM module, supporting the ITU J83-A/B/C standard
- Multi TS processing simultaneously
- TS interface for Full Band Capture device
- Various descrambling algorithms of the DVB

Security Processing

- Advanced CA
- Downloadable Conditional Access System
- TVOS security mechanism
- Secure boot, secure storage, and secure upgrade
- DRM and hardware watermark
- HDCP 2.2/1.4 protection for HDMI outputs

Graphics and Display Processing (Imprex 2.0 Processing Engine)

- Dolby Vision, HDR10, HLG, and SLF
- Conversion from HDR to SDR
- Image enhancement algorithms
- Hardware overlaying of multi-channel graphics and video inputs
- Multiple graphics layers and video layers
- Multi-order vertical and horizontal scaling of videos and graphics; free scaling
- Screen mirroring and video rotation
- Full-format 3D video processing and display
- Enhanced TDE
- Anti-aliasing, anti-flicker, enhancement of image colors and luminance, NR, DEI, sharpening, as well as adjustment of the luminance, chrominance, contrast, and saturation
- Ultra-low-delay video processing

Audio and Video Interfaces

- 4K@60 fps/50 fps/30 fps/25 fps, 1080p@60 fps/50 fps/30 fps/24 fps, 1080i@60 fps/50 fps, and 720p/576p/576i/480p/480i outputs
- PAL, NTSC, and SECAM standard outputs, and forcible standard conversion
- Aspect ratio of 4:3 or 16:9, forcible aspect ratio conversion, and free scaling
- HD and SD outputs
- One HDMI 2.0a TX with HDCP 2.2 output, supporting maximum 4K x 2K@60 fps resolution
- Analog video interfaces
 - One CVBS interface
 - One YPbPr interface (optional)
 - Four internal VDACS
 - VBI
- Audio interface
 - Audio-left and audio-right outputs
 - S/PDIF interface



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- One internal ADAC
- 1-channel I²S or PCM digital audio input or output
- HDMI audio output

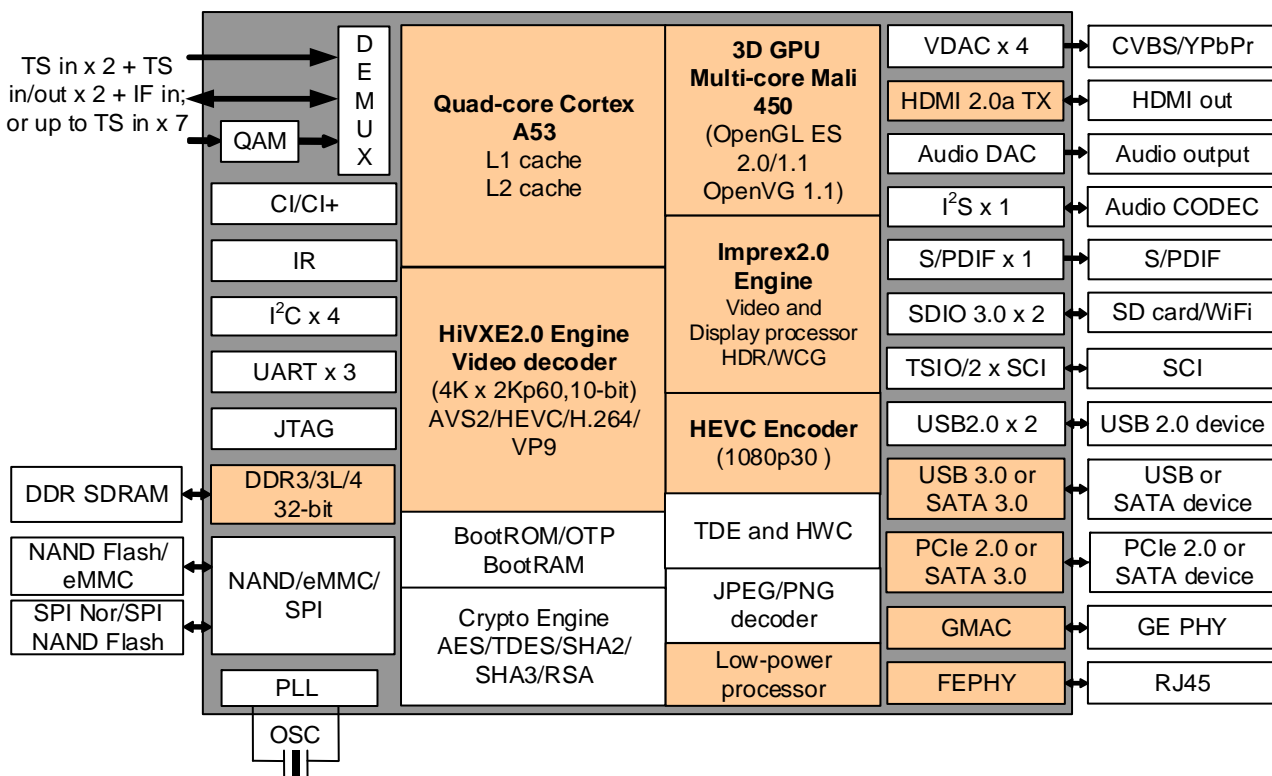
Peripheral Interfaces

- Two USB 2.0 host ports
- PCIe 2.0, USB 3.0, and SATA 3.0 interfaces (optional; the SATA 3.0 interface is multiplexed with the PCIe 2.0 or USB 3.0 interface.)
- One FE port (with internal PHY) and one GE port (RGMII)
- Two 4-bit SDIO 3.0 interfaces
- Three UART interfaces
- Two SCIs
- One CI/CI+ interface

- One TSIO interface
- One IR receiver
- One LED and keypad control interface
- Four I²C interfaces
- Multiple groups of GPIO interfaces
- One embedded POR

Others

- Various boot modes
- Boot program downloading and execution over a serial port or USB port
- Passive standby low-power design, Integrated dedicated standby processor, supporting various low-power modes
- BGA package, supporting the 2-layer PCB

Functional Block Diagram

Hi3796M V200 is a full-4K high-performance SoC for the DVB STB market. It integrates the quad-core 64-bit high-performance Cortex A53 processor and multi-core high-performance 2D/3D acceleration engine. Besides, it supports AVS2/H.265/VP9 4K x 2K@P60 10-bit ultra-HD video decoding, high-performance H.265/H.264 HD video encoding, HDR video decoding and display, Dolby, and DTS audio processing. Hi3796M V200 also provides rich internal peripheral interfaces, such as USB 2.0, USB 3.0, SDIO 3.0, SATA, and PCIe 2.0 interfaces; It supports TVOS/Android/Linux OSes. These features help customers implement full-4K service deployment, and enable Hi3796M V200 to provide the best user experience in the industry in aspects of picture quality, stream compatibility, video playing smoothness, and STB performance and meet the requirements of continuously increasing value-added services such as video communication, karaoke, cloud game, and multi-screen interaction.

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- The use of Real 8/9/10 decoding in this document has obtained permission from RealNetworks, Inc.

Acronyms and Abbreviations

AAC-LC	advanced audio coding low complexity
ADAC	audio digital-to-analog converter
AES	Advanced Encryption Standard
AMR-NB	adaptive multi-rate narrowband
AMR-WB	adaptive multi-rate wideband
APE	Monkey's Audio
AVC	advanced video coding
AVS	Audio Video Standard/adaptive voltage scaling
BGA	ball grid array
CA	conditional access
CBR	constant bit rate
CI	common interface
CSC	color space conversion
CVBS	composite video broadcast signal
DD	Dolby Digital
DDR	double data rate
DEI	de-interlacing
DES	Data Encryption Standard
DRM	digital rights management
DSP	digital signal processor
DTS	Digital Theater Systems
DVB	Digital Video Broadcasting
DVB-C	Digital Video Broadcasting-Cable
DVB-CSA	Digital Video Broadcasting-common scrambling algorithm
DVFS	dynamic voltage and frequency scaling
ECC	error checking and correction
eMMC	embedded multimedia card
FE	fast Ethernet

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FLAC	free lossless audio codec
GE	gigabit Ethernet
GFLOPS	giga floating-point operations per second
GMC	global motion compensation
GPIO	general-purpose input/output
GPU	graphics processing unit
HD	high definition
HDCP	High-bandwidth Digital Content Protection
HDMI	high definition multimedia interface
HDR	high dynamic range
HE-AAC	high-efficiency advanced audio coding
HEVC	high efficiency video coding
HLG	Hybrid Log-Gamma
IF	intermediate frequency
I ² C	inter-integrated circuit
I ² S	inter-IC sound
IR	infrared
ITU	International Telecommunication Union
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group
LED	light emitting diode
MLC	multi-level cell
MPEG	Moving Picture Experts Group
MTri/s	million triangles per second
MVC	multiview video coding
NR	noise reduction
NTSC	National Television System Committee
PAL	phase alternating line
PCB	printed circuit board
PCIe	Peripheral Component Interconnect Express
PCM	pulse code modulation
PID	packet identifier



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PNG	portable network graphics
POR	power-on reset
QAM	quadrature amplitude modulation
RGMII	reduced gigabit media independent interface
ROI	region of interest
SATA	Serial Advanced Technology Attachment
SCI	smart card interface
SD	standard definition
SDIO	secure digital input/output
SDR	single data rate
SECAM	sequential color with memory
SLC	single-level cell
SoC	system on chip
S/PDIF	Sony/Philips Digital Interface Format
SPI	serial peripheral interface
STB	set-top box
SVP	secure video path
TDE	two-dimensional engine
TEE	Trusted Execution Environment
TS	transport stream
TSIO	Smart Card Transport IO
TX	transmit
UART	universal asynchronous receiver transmitter
VBI	vertical blanking interval
VBR	variable bit rate
VDAC	video digital-to-analog converter