



Hi3516C V300 Professional HD IP Camera SoC

Brief Data Sheet

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Key Specifications

Processor Core

ARM926@800 MHz with 32 KB I-cache and 32 KB D-cache

Video Encoding

- H.264 BP/MP/HP
- H.265 Main Profile
- MJPEG/JPEG baseline

Video Encoding Performance

- Maximum 2-megapixel resolution for H.264/H.265 encoding
- Real-time multi-stream H.264/H.265 encoding capabilities
 - 1920x1080@45 fps
 - 1920x1080@30 fps+720x480@30 fps+360x240@30 fps
- JPEG snapshot at 2 megapixels@5 fps
- CBR, VBR, FIXQP, AVBR, and QMAP modes
- Maximum 30 Mbit/s output bit rate
- Encoding of eight ROIs

Intelligent Video Analysis

Integrated IVE, supporting various intelligent analysis applications such as motion detection, perimeter defense, and video diagnosis

Video and Graphics Processing

- 3DNR, image enhancement, and DCI
- Anti-flicker for output videos and graphics
- 1/15x to 16x video and graphic scaling
- Overlaying of video and graphics
- Picture rotation by 90°, 180° or 270°
- Picture mirroring and flipping
- OSD overlaying of eight regions before encoding

ISP

- 3A (AE, AF, and AWB) function. The third-party 3A algorithms are supported.
- FPN removal and DPC
- LSC, LDC, and purple edge correction
- Direction-adaptive demosaic
- Gamma correction, DCI, and color management and enhancement
- Adaptive region de-fog
- Multi-level NR (BayerNR and 3DNR) and sharpening enhancement
- Local tone mapping
- Sensor built-in WDR and 2F WDR (line-base/frame-base/DCG)
- DIS
- ISP tuning tools for the PC

Audio Encoding/Decoding

- Voice encoding/decoding complying with multiple protocols by using software
- Compliance with the G.711, G.726, and ADPCM protocols

- Audio 3A functions (AEC, ANR, and AGC)

Security Engine

- Various encryption and decryption algorithms implemented by using hardware, including AES, DES, 3DES, and RSA
- HASH (SHA1/SHA256/HMAC_SHA/HMAC_SHA256) algorithms implemented by using hardware
- Integrated 512-bit OTP storage space and random number generator

Video Interfaces

- VI interfaces
 - 8-/10-/12-/14-bit RGB Bayer DC timing VI
 - BT.601, BT.656, and BT.1120 VI interfaces
 - MIPI, LVDS/sub-LVDS, and HiSPi
 - Compatibility with mainstream HD CMOS sensors provided by Sony, ON, OmniVision, and Panasonic
 - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
 - Programmable sensor clock output
 - Maximum input resolution of 2048 x 2048, up to 198 megapixels/s
- VO interfaces
 - One PAL/NTSC output for automatic load detection
 - One BT.656 VO interface
 - 6-bit RGB565 serial LCD output

Audio Interfaces

- Integrated audio CODEC supporting 16-bit audio inputs and outputs
- Mono-channel differential MIC inputs for reducing the background noises
- Single-ended dual-channel input
- I²S interface for connecting to the external audio CODEC

Peripheral Interfaces

- POR
- One integrated high-precision RTC
- Integrated 3-channel LSADC
- Three UART interfaces (including one 4-wire interface)
- IR, I²C, SPI, and GPIO interfaces
- Four PWM interfaces
- Two SDIO 2.0 interfaces, supporting the 3.3 V level and 1.8 V level
- One USB 2.0 host/device port
- RMII in 10/100 Mbit/s full-duplex or half-duplex mode, TSO network acceleration, and PHY clock output

External Memory Interfaces

- SDRAM interface
 - 16-bit DDR3/DDR3L interface with the maximum capacity of 4 Gbits
- SPI NOR flash interface
 - 1-/2-/4-wire mode
 - Maximum capacity of 32 MB
- SPI NAND flash interface with maximum 4 Gbits capacity



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- SD card interface supporting the maximum capacity of 2 TB
- eMMC 4.5 interface with 4-bit data width

Boot

- Booting from the SPI NOR flash, SPI NAND flash, or eMMC
- Secure boot

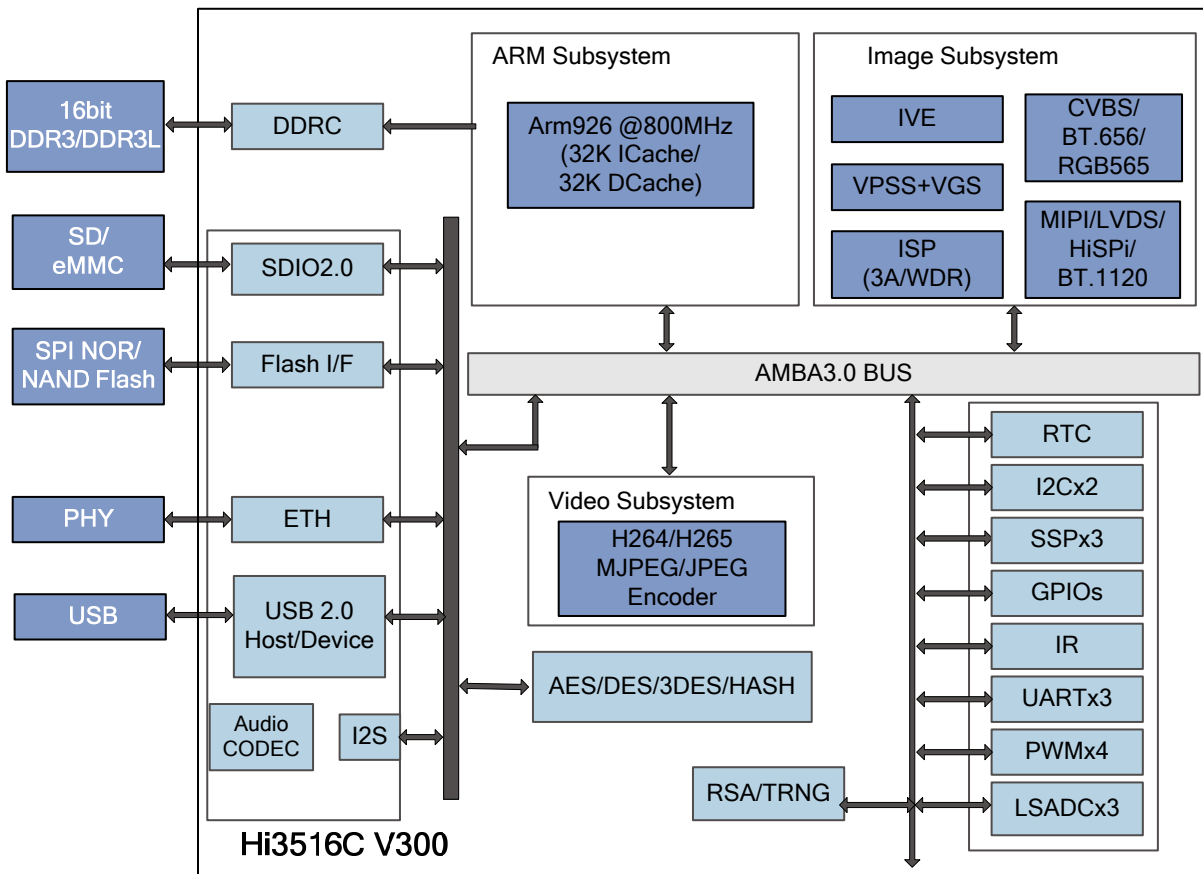
SDK

- Linux-3.18-based SDK
- High-performance H.264 PC decoding library
- High-performance H.265 PC/Android/iOS decoding library

Physical Specifications

- Power consumption
 - 1080p30, typical power consumption of 550 mW
 - Deep standby wakeup
- Operating voltages
 - 0.9 V core voltage
 - 3.3 V±10% I/O voltage
 - 1.35 V or 1.5 V DDR3/3L SDRAM interface voltage
- Package
 - Body size of 12 mm x 12 mm (0.47 in. x 0.47 in.), 0.65 mm (0.03 in.) ball pitch, TFBGA RoHS package with 273 pins

Functional Block Diagram

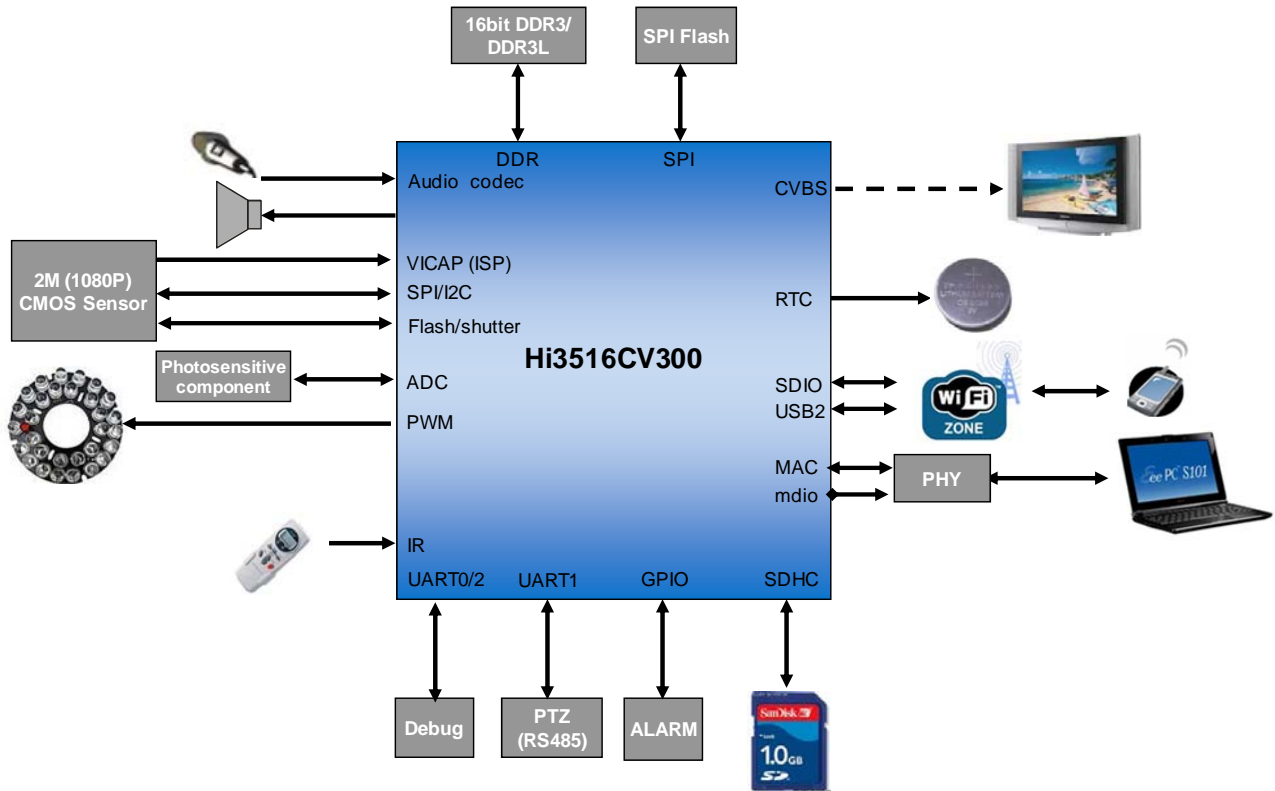


Hi3516C V300 is a new-generation SoC designed for the industry-dedicated HD IP camera. It has an integrated new-generation ISP and the latest H.265 video compression encoder in the industry. It uses the advanced low-power technology and architecture design. All of these features enable Hi3516C V300 to lead the industry in the low bit rate, high profile, and low power consumption. Hi3516C V300 integrates the POR, RTC, audio CODEC, and standby wakeup circuit, which significantly reduces customers' EBOM cost. In addition, the interface design similar to that of other HiSilicon DVR and NVR chips facilitate development and mass production of customer's products.



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Hi3516C V300 HD IP Camera Solution





Acronyms and Abbreviations

3DES	Triple Data Encryption Standard
ADPCM	adaptive differential pulse code modulation
AE	automatic exposure
AEC	acoustic echo cancellation
AES	Advanced Encryption Standard
AF	automatic focus
ALC	automatic level control
ANR	audio noise reduction
AVBR	adaptive variable bit rate
AWB	automatic white balance
CBR	constant bit rate
CMOS	complementary metal-oxide-semiconductor
CODEC	coder/decoder
DC	direct current
DCI	dynamic contrast improvement
DDR	double data rate
DES	Data Encryption Standard
DIS	digital image stabilization
DNR	digital noise reduction
DPC	defect pixel correction
DVR	digital video recorder
EBOM	engineering bill of materials
eMMC	embedded multimedia card
FPN	fixed pattern noise
GPIO	general-purpose input/output
HD	high definition
HiSPi	high-speed serial pixel interface
I ² C	inter-integrated circuit
I ² S	inter-IC sound
IR	infrared

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ISP	image signal processor
IVE	intelligent video engine
LCD	liquid crystal display
LDC	lens distortion correction
LSC	lens shading correction
LVDS	low voltage differential signal
MIC	microphone
MIPI	mobile industry processor interface
NR	noise reduction
NTSC	National Television System Committee
NVR	network video recorder
OSD	on-screen display
OTP	one-time programmable
PAL	phase alternating line
POR	power-on reset
PWM	pulse-width modulation
RMII	reduced media independent interface
RoHS	Restriction of Hazardous Substances
ROI	region of interest
RSA	Rivest-Shamir-Adleman
RTC	real-time clock
SAR ADC	successive approximation register analog-to-digital converter
SDHC	Secure Digital High Capacity
SDIO	secure digital input/output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SoC	system-on-chip
SPI	serial peripheral interface
TFBGA	thin & fine ball grid array
TSO	TCP segmentation offload
UART	universal asynchronous receiver transmitter
VBR	variable bit rate



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VGA	video graphics array
VI	video input
VO	video output
WDR	wide dynamic range