

Hi3798M V100 Brief Data Sheet

Key Specifications

CPU

- Quad-core ARM Cortex A7, up to 1.5 GHz dominant frequency
- Integrated multimedia acceleration engine NEON
- Hardware Java acceleration
- Integrated hardware floating-point coprocessor

3D GPU

- Quad-core Mali450
- OpenGL ES 2.0/1.1/1.0 OpenVG 1.1, EGL

Memory Interfaces

- DDR3/DDR3L interface
 - Maximum 2 GB capacity
 - 32-bit memory
 - Maximum 800 MHz frequency (DDR-1600)
- NAND flash interface
 - SLC/MLC flash memory
 - 8-bit data width
 - Maximum 64 GB capacity
 - Maximum 64-bit ECC
- eMMC/tSD/fSD flash memory

HiVXE Video Decoding

- H.265 Main Profile@L5.0 High-tie
- H.264 BP/MP/HP@L5.1
- Full-HD 3D videos (MVC), blu-ray navigation
- AVS baseline profile @L6.0, AVS-P16 (AVS+)
- MPEG1
- MPEG2 SP@ML, MP@HL
- MPEG4 SP@L0-3, ASP@L0-5, GMC
- MPEG4 short header format (H.263 baseline)
- VC-1 SP@ML, MP@HL, AP@L0-3
- VP6/8
- 4K x 2K@30 fps decoding
- Low delay decoding
- Simultaneous 4-channel HD decoding

Image Decoding

- Full HD JPEG hardware decoding, maximum 64 megapixels
- MJPEG decoding, maximum 1080p@40 fps
- PNG hardware decoding, maximum 64 megapixels

Video and Image Encoding

- H.264 BP/MP/HP@L4.2 video encoding, 1080p@30 fps
- JPEG hardware encoding, maximum 1080p@30 fps
- VBR or CBR mode for video encoding
- Low delay encoding

Audio Encoding and Decoding

- MPEG L1/L2
- Dolby Digital/Dolby Digital Plus Decoder-Converter
- Dolby True HD decoding
- DTS and DTS HD core decoding

- Dolby Digital/DTS transparent transmission
- AAC-LC and HE AAC V1/V2 decoding
- APE, FLAC, Ogg, AMR-NB, and AMR-WB decoding
- G.711 (u/a) audio decoding
- Downmixing, resampling, highly dynamic volume control
- High-quality Karaoke, supporting echo cancellation and G.711v (u/a), AMR-NB, AMR-WB, and AAC-LC audio encoding

Image and Display Processing (Imprex Processing Engine)

- Hardware overlaying of multi-channel graphics and video inputs
- Three OSD layers
- Four video layers
- Screen mirroring
- Ultra-low-delay video processing
- Letter box and PanScan
- Full format 3D video processing and display
- Multi-tap vertical and horizontal scaling of videos and graphics; free scaling
- Enhanced full-hardware TDE
- Full-hardware anti-aliasing and anti-flicker
- CSC with configurable coefficients
- Image enhancement and denoising
- Deinterlacing
- Sharpening
- Chrominance, luminance, contrast, and saturation adjustment
- Video Db/Dr processing

Audio/Video Interfaces

- PAL, NTSC, and SECAM standard output, and forcible standard conversion
- Aspect ratio of 4:3 or 16:9 and forcible aspect ratio conversion
- 4K x 2K/1080p50/1080p30/1080p24/1080i60/1080i50 /720p/576p/576i/480p/480i output
- One SD output and one HD output from the same source or different sources
- One HDMI 1.4a TX with HDCP 1.4 output
 - Analog video interfaces
 - One CVBS interface
 - One embedded VDAC
- Audio interfaces
 - Audio-left and audio-right channels
 - SPDIF interface
 - Embedded ADAC output
 - One I²S/PCM digital audio input/output (Optional)
 - HDMI audio output

Peripheral Interfaces

• One USB 3.0 host port (Optional)



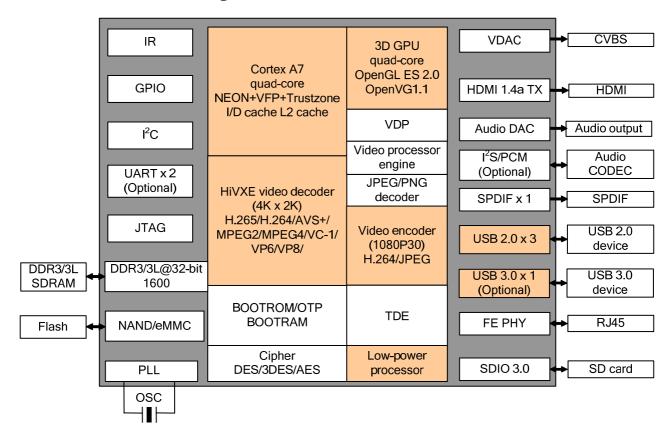
Hi3798M V100 Brief Data Sheet

- Three USB 2.0 host ports
- Boot and debugging over the USB port
- One SDIO 3.0 interface
- One 10 Mbit/s or 100 Mbit/s adaptive Ethernet port with the integrated FE PHY
- One IR receiver with one input interface
- Multiple I²C interfaces
- Multiple UART interfaces (Optional)
- Multiple GPIO interfaces
- Integrated POR module

Other Specifications

- Embedded secure boot module, supporting anti-ROM-flashing
- Secure video path
- 2-layer PCB design
- Various boot modes
- USB bootstrap when the flash memory is empty
- Integrated standby processor, supporting various standby modes and less than 30 mW standby power consumption
- Low-power design such as AVS and DVFS

Functional Block Diagram



Hi3798M V100 is a cost-effective chip solution targeted at the over-the-top (OTT) STB market. It brings the best user experience in the industry in terms of stream compatibility, smoothness and picture quality of live video playback, and STB performance. With an integrated high-performance quad-core processor and embedded NEON, Hi3798M V100 meets differentiated service requirements. It also supports Dolby and DTS audio processing. To meet the growing requirements on multimedia playback, video communication, and multi-screen transcoding, Hi3798M V100 supports HD video decoding in various formats (including H.265, H.264, AVS+, MVC, MPEG2, MPEG4, VC-1, VP6, and VP8) and high-performance H.264 encoding. Hi3798M V100 provides a smooth man-machine interface and rich gaming experience with a high-performance multi-core 2D/3D acceleration engine. It also enables flexible connection schemes with one Ethernet port, three USB 2.0 ports, one USB 3.0 port(Optional), and more peripheral interfaces.

Ⅲ NOTE

- DTS, mentioned in this document, is a registered trademark of DTS Inc. and its subsidiaries. Any parties intending to use the trademark must obtain the permission from DTS Inc. or its subsidiaries.
- Dolby, mentioned in this document, is a registered trademark of Dolby Laboratories, Inc. Any
 parties intending to use the trademark must obtain the permission from Dolby Laboratories, Inc.



Hi3798M V100 Brief Data Sheet

Acronyms and Abbreviations

ADAC audio digital-to-analog converter

ADB Android debug bridge AVS adaptive voltage scaling

BGA ball grid array
CBR constant bit rate
CSC color space conversion

CVBS composite video broadcast signal

DSP digital signal processor

DVFS dynamic voltage frequency scaling

ECC error correcting code eMMC embedded multimedia card

FE fast Ethernet

GMC global motion compensation
GPIO general-purpose input/output
GPU graphics processing unit

HDMI high-definition multimedia interface
HEVC high efficiency video coding
I²C inter-integrated circuit

IR infrared I²S inter-IC sound

JPEG Joint Photographic Experts Group
MJPEG Motion Joint Photographic Experts Group

MLC multi-level cell

MPEG Moving Picture Experts Group MVC multiview video coding

NTSC National Television System Committee

OTT over-the-top
PCB printed circuit board
PCM pulse-code modulation
POR power-on reset

POR power-on reset
ROI region of interest
SDIO secure digital input/output

SLC single-level cell

SPDIF Sony/Philips digital interface SPI serial peripheral interface SSVP super secure video path

STB set-top box

TDE two-dimensional engine

UART universal asynchronous receiver transmitter

VBI vertical blanking interval

VBR variable bit rate

VDAC video digital-to-analog converter

www.hisilicon.com Date: 2016-10-16