Preliminary Data Sheet

MS1153/MS1193

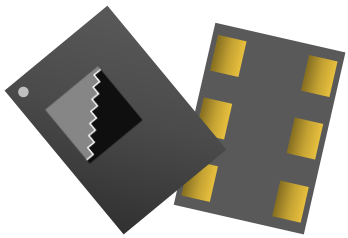
Dual Frequency Ultra-Low Phase Jitter Digitally Synthesized Oscillators (DSO)

Features

- Factory Programmable
  - Any frequency from 20 MHz to 2200 MHz
  - Differential Output: CML/LVDS/LVPECL/LVDS-EXT/HCSL
- Ultra-Low RMS phase jitter (12 KHz to 20 MHz)
  - 22 fs at 312.50 MHz
  - 22 fs at 491.52 MHz
  - 20 fs at 625 MHz
  - 22 fs at 1250 MHz
- Total stability of ±20 ppm
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jumps
- FS Pin: Supports 2 Frequencies
- Standard 2.5X2.0 mm, 2.0X1.6 mm 6-pin LGA package
- 1.8V supply with internal regulator
- Superior power supply immunity
- Industrial Temperature range: -40°C to 85°C
- Extended Temperature range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

Applications

- Network Equipment (Optical Modules, routers)
- 100G/200G/400G/800G/1.6T/3.2T OTN, Coherent optics
- Storage, switches, servers, NICs, accelerators
- 3G to 24G SDI broadcast video
- 10G/40G/100G optical ethernet
- 112G/224G/448G PAM4 Clocking
- Test and measurement equipment



General Description

The MS1153/MS1193 is a digitally synthesized oscillator (DSO) that combines advanced Bulk Acoustic Wave (BAW) resonator technology with high-performance digital frequency synthesis to deliver highly stable, fully programmable multi-GHz clocks with extremely low phase Jitter.

Built-in Adaptive Intelligence continuously monitors operating conditions in the background, using autonomous DSP algorithms to maintain robust and consistent performance across process, voltage, and temperature.

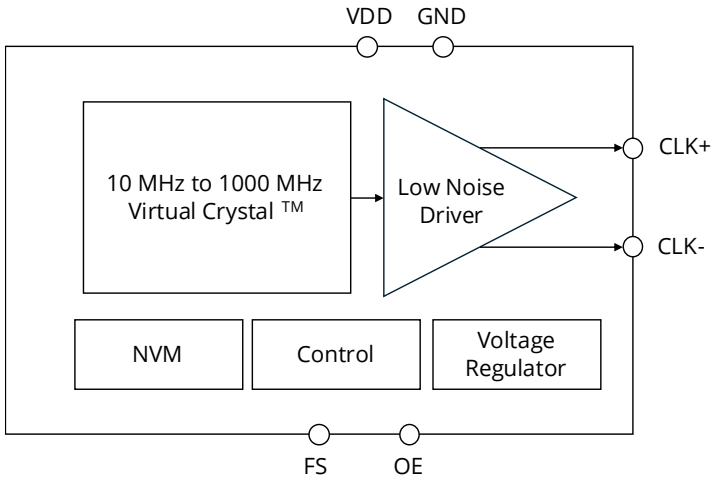
The devices are factory programmed to provide an accurate frequency between 20 MHz and 2200 MHz at less than 1 ppb resolution.

The MS1153/MS1193 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry.

Device Information

Part Number	Package	Description
MS1153	2.5x2.0 mm 6-pin LGA	Dual Freq Oscillator
MS1193	2.0x1.6 mm 6-pin LGA	Dual Freq Oscillator

Figure 1. Functional Block Diagram



MS1153/MS1193

Pin Assignment and Pin Description (TOP VIEW)

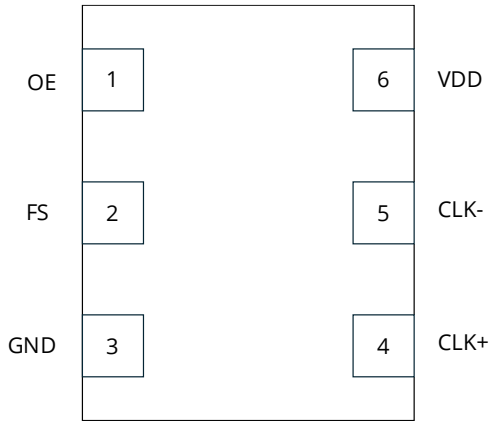


Figure 2. MS1153/MS1193 Pin Assignments

Table 1. MS1153/MS1193 Pin Descriptions

Pin No	Name	Description
1	OE	Output Enable • High/Floating: Output enabled (Internal pull-up of 100kΩ) • Low: Output disabled
2	FS	Frequency Select FS=1 or NC: Frequency 1 FS=0: Frequency 2
3	GND	Ground
4	CLK+	True Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply – connect bypass capacitor between this pin and pin 3. Keep bypass as close as possible to the pins

Part Ordering Information

Figure 3 shows a logic tree for ordering each of the available parts.

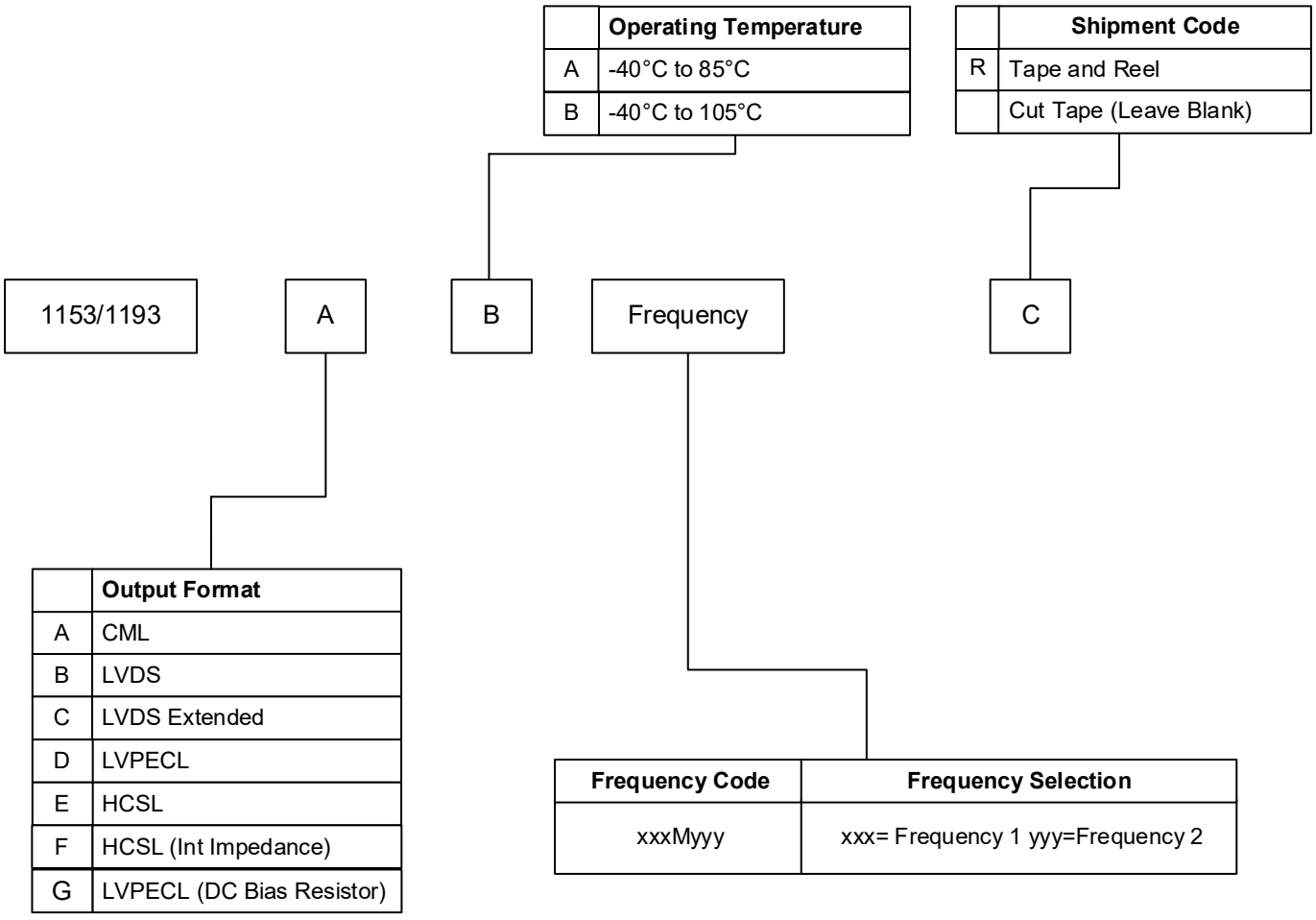


Figure 3. MS1153/MS1193 Part Ordering Information

Table 2. Example of ordering part number

Base P/N	Output Format	Operating Temperature	Frequency Code 1	Frequency Code 2	Shipment Type	**Ordering part number**
1153	HCSL	-40°C to 85°C	156.25 MHz	312.5MHz	Tape and Reel	**1153EA156M312R**
1193	LVPECL	-40°C to 105°C	312.5 MHz	625MHz	Tape and Reel	**1193DB312M625R**

Input Frequency codes for ordering

Code (xxx/yyy)	Frequency (MHz)
010	10
100	100
106	106.25
122	122.88
153	153.6
156	156.25
212	212.5
245	245.76
250	250
307	307.2
312	312.5
322	322.2656525
491	491.52
500	500
614	614.4
625	625
644	644.53125
750	750
983	983.05
C50	1250

Please contact Mixed-Signal Devices for additional frequency codes

Specifications

Table 3. Electrical Specifications

Typical values are specified at T_A= 25°C, V_{DD}=1.8V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard output terminations (See Figure 9-15). A 0.1uF and 10uF bypass capacitors should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Frequency Range						
Frequency Range	F_{CLK}	All Output Formats	20		2200	MHz
Frequency Stability						
Frequency Stability*	F_{STB}		-20		20	PPM
*Frequency stability includes initial tolerance, voltage tolerance, operating temperature and aging (10 year, +25°C). Aging is estimated from environmental reliability tests;						
Clock Output Jitter Characteristics						
RMS Phase Jitter (12 KHz – 20 MHz integration band)	Φ_{JITTER}	Frequency=491.52 MHz		22	33	fs
		Frequency=625 MHz		20	30	fs
Note: Phase jitter measured on Agilent 5052B Signal Source Analyzer						
Operating Voltage/Temperature Range						
Supply Voltage	V_{DD}		1.71 (-5%)	1.8	1.89 (+5%)	V
Temperature Range	T_A	Industrial Temperature	-40	25	85	°C
		Extended Industrial Temperature	-40	25	105	°C

Current Consumption

Supply Current Consumption	I_{DD}	LVDS Output (Output Enabled)		150	180	mA
		All Other Outputs (Output Enabled)		160	190	mA
		Tristate Hi-Z (Output Disabled. OE=0)		70	84	mA

Input Characteristics

Digital Input Levels(OE/FS)	V_{IH}		$0.7XV_{DD}$			V
	V_{IL}				$0.3XV_{DD}$	V
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10 Char data	ms

PSRR Characteristics

Power Supply-Induced Phase Noise	PSPN	Spurs induced by 50mV power supply ripples (1) (Center Frequency is 312.5MHz)		-110		dBc
Power Supply-Jitter Sensitivity	PSJS			0.2		fs/mV

Note:

(1) Measured with 50 mVpp ripple from 500 KHz to 10 MHz applied on VDD Pin

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps
CML Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 9, Figure 10	0.6	0.8	1	V
LVDS Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 11	0.5	0.7	0.9	V
LVDS-EXT Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 11	0.8	1.2	1.6	V
LVPECL Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 12, Figure 13	1.2	1.4	1.6	V
HCSL Output (AC or DC-Coupled)	Vpp	Differential Pk-Pk See Figure 14, Figure 15	1.1	1.35	1.6	V
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV

Unless otherwise specified, all differential output amplitudes are measured across a 100 Ω differential load or the termination network shown in the referenced output driver figures on the following pages

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O (OE/FS)	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Junction Temperature		150	°C
Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.			

Table 5. Environmental Compliance

Parameter	Test Condition	Value	Unit
Moisture Sensitivity Level (MSL)	MSL3 @260°C		
Soldering Temperature	MIL-STD-883, Method 2003	260	°C
Electrostatic Discharge (HBM)	JEDEC JS-001	2000	V
Charge-Device Model (CDM)	JEDEC JESD22-C101	500	V
Latch-up Compliance	JESD78 Compliant		

Table 6. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
2.5mm x 2mm 6 pin LGA	Maximum Board Temperature	T_B	125	°C
	Thermal Resistance, Junction to Ambient	$ø_{JA}$	90	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	40	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C
Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.				

Table 7. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
2.0mm X 1.6mm 6 pin LGA	Maximum Board Temperature	T_B	125	°C
	Thermal Resistance, Junction to Ambient	$ø_{JA}$	110	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	60	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C
Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.				

Table 8. Typical Output Phase Noise Characteristics
VDD= 1.8V, T_A = 25°C, Output Type = LVDS-EXT

Offset frequency	312.5 MHz	491.52 MHz	625 MHz	1250 MHz	Unit
1 KHz	-103	-98	-99	-93	dBc/Hz
10 KHz	-132	-130	-127	-122	dBc/Hz
100 KHz	-154	-152	-149	-143	dBc/Hz
1 MHz	-164	-160	-159	-152	dBc/Hz
10 MHz	-165	-161	-160	-151	dBc/Hz
20 MHz	-166	-161	-160	-153	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	22	22	20	22	fs

Typical Output Measured Phase Noise Plots

This section shows MS1153/MS1193 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = LVDS-EXT.

The plots were captured using an Agilent E5052B Signal Source Analyzer.

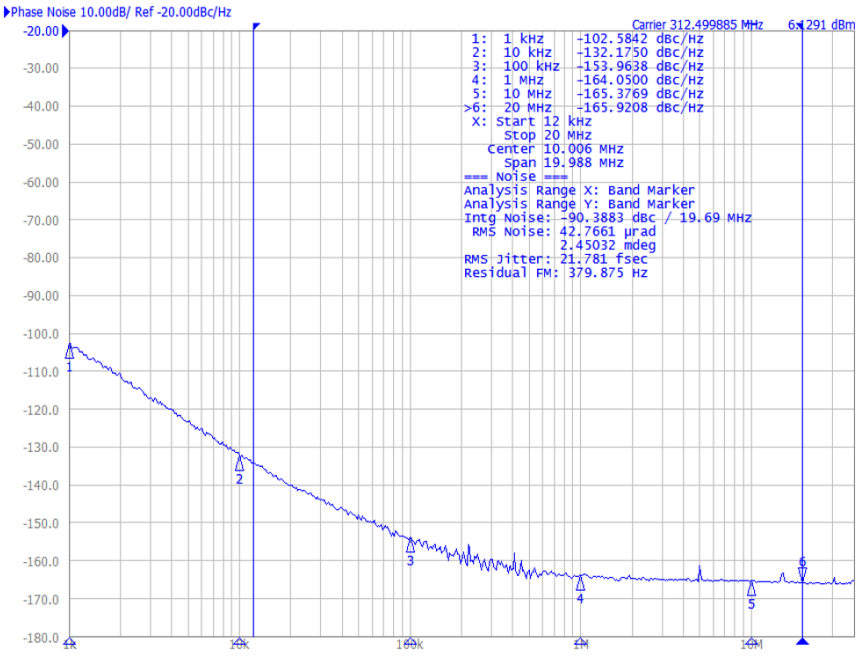


Figure 4. Center Frequency: 312.5 MHz

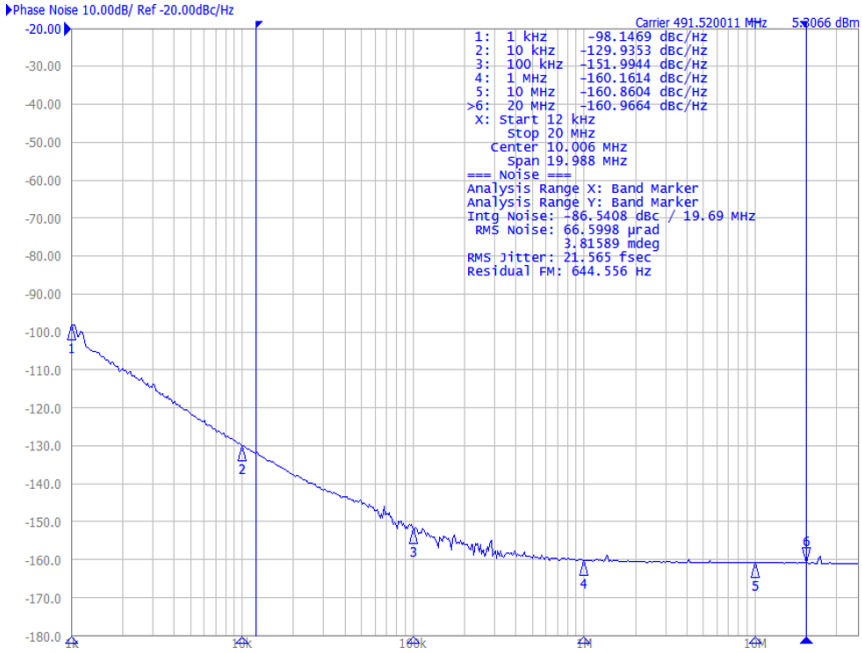


Figure 5. Center Frequency: 491.52 MHz

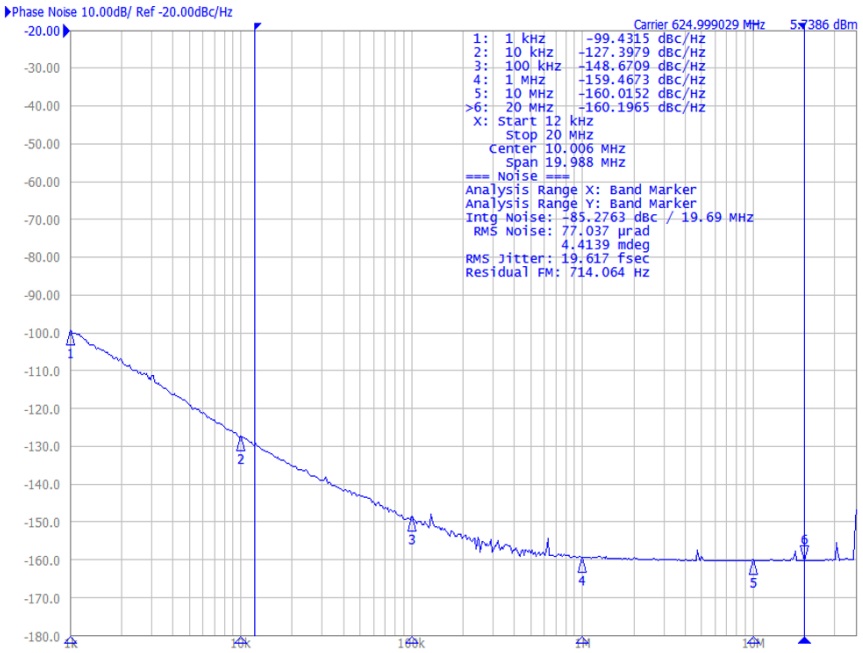


Figure 6. Center Frequency: 625 MHz

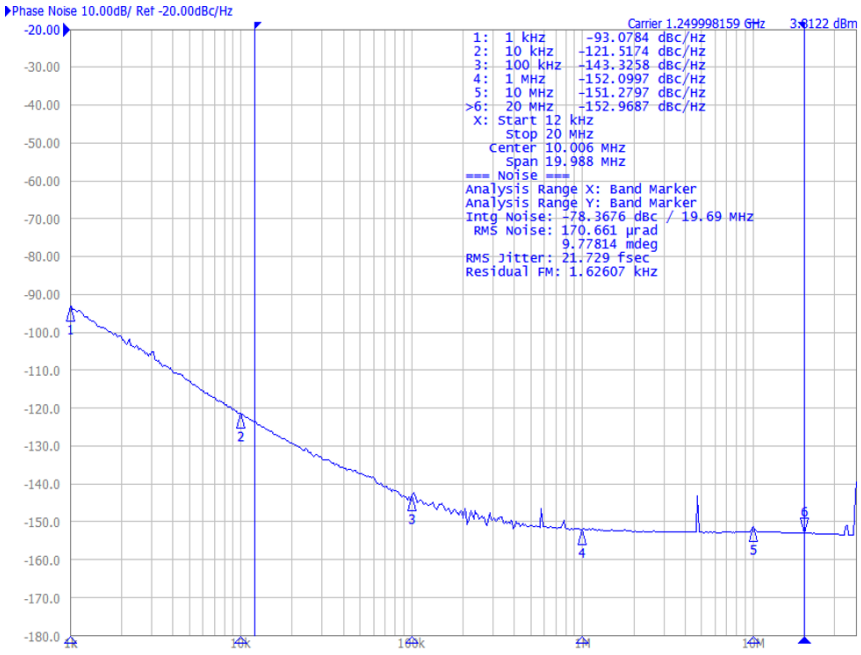


Figure 7. Center Frequency: 1250 MHz

Output Terminations

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff
LVDS	0.7V	AC	100 Ω diff
LVDS-EXT	1.2V	AC	100 Ω diff
LVPECL	1.4V	AC	50 Ω to VT
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT
HCSL (Int Term)	1.35V	AC or DC	None
HCSL	1.35V	DC	50 Ω to GND

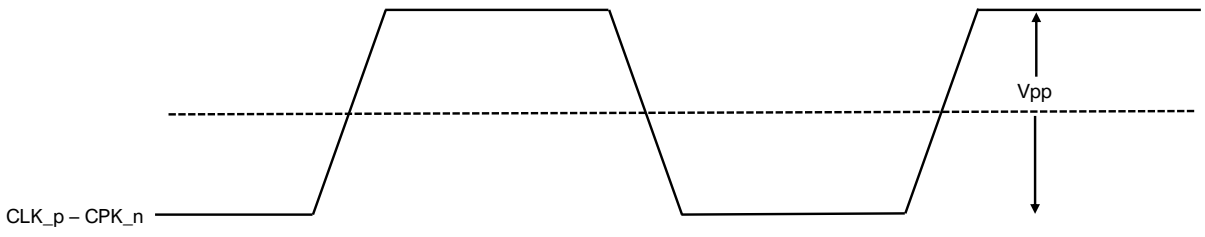


Figure 8. Differential Output Swing

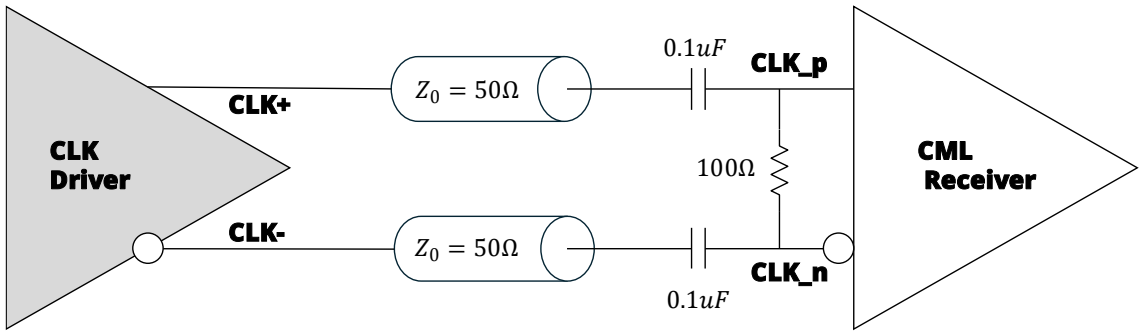


Figure 9. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

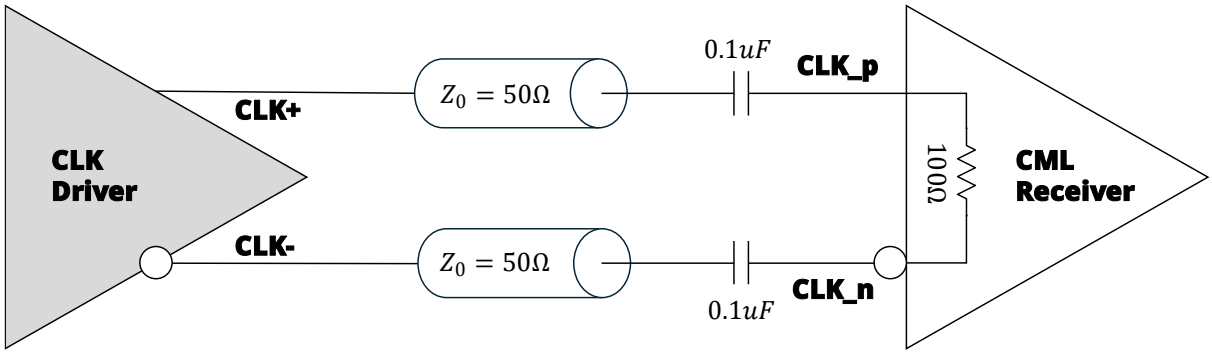


Figure 10. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

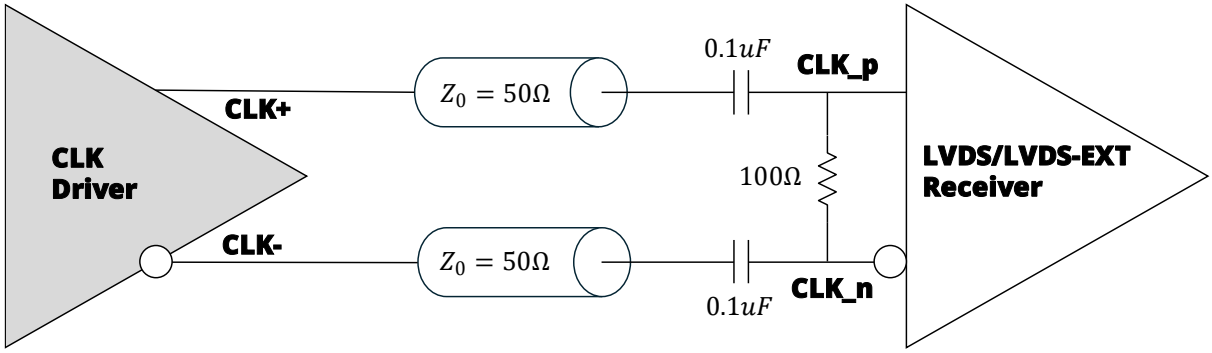


Figure 11. LVDS/LVDS-EXT Output Driver with 100 Ω Differential Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVDS/LVDS-EXT	0.7V/1.2V	AC	100 Ω diff

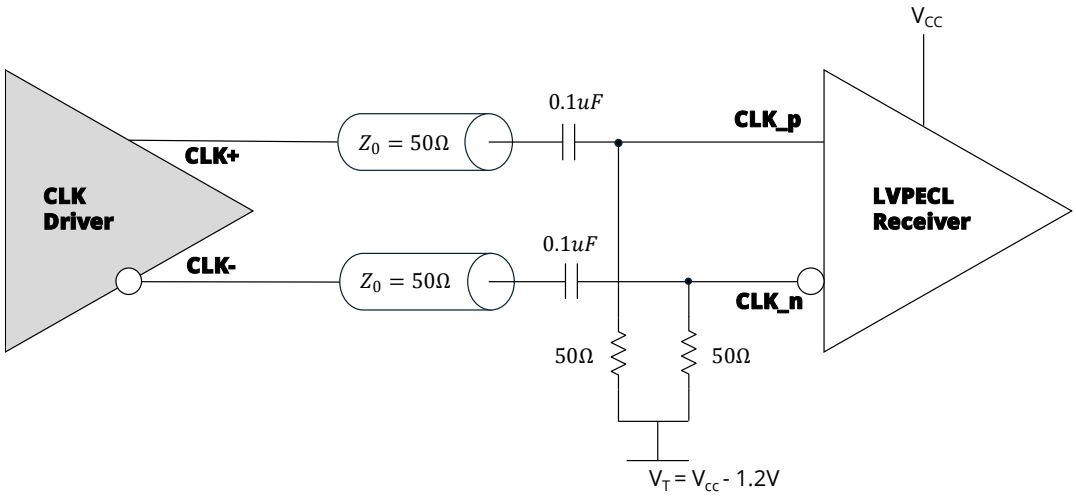


Figure 12. LVPECL Output Driver with External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL	1.4V	AC	50Ω to VT

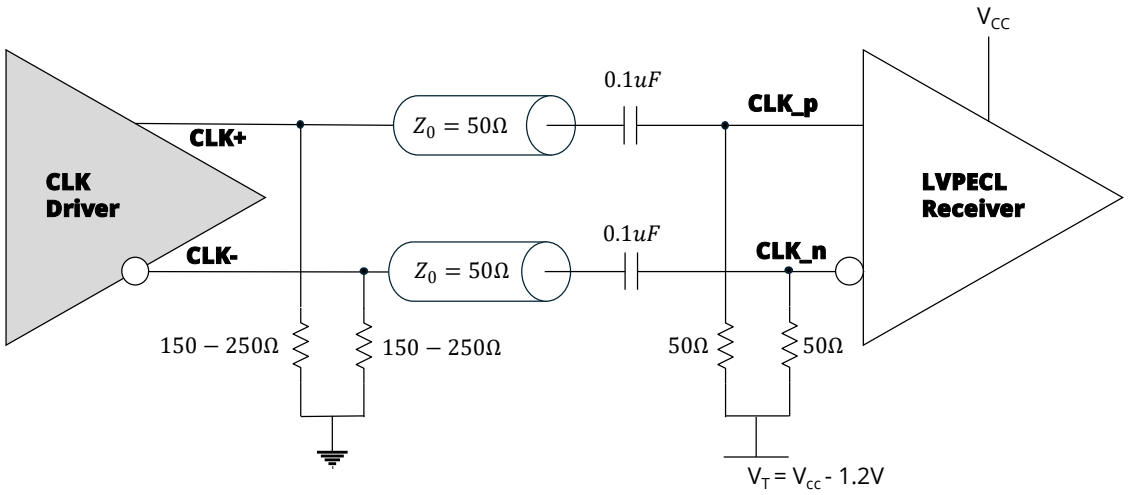


Figure 13. LVPECL Output Driver with Source Bias Resistors and External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT

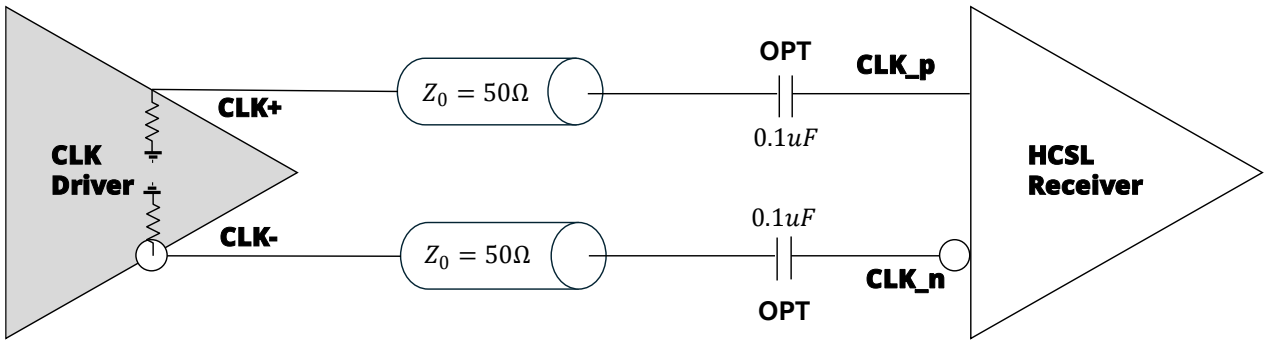


Figure 14. HCSL Output Driver with Integrated Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL (Int Term)	1.35V	AC/DC	None

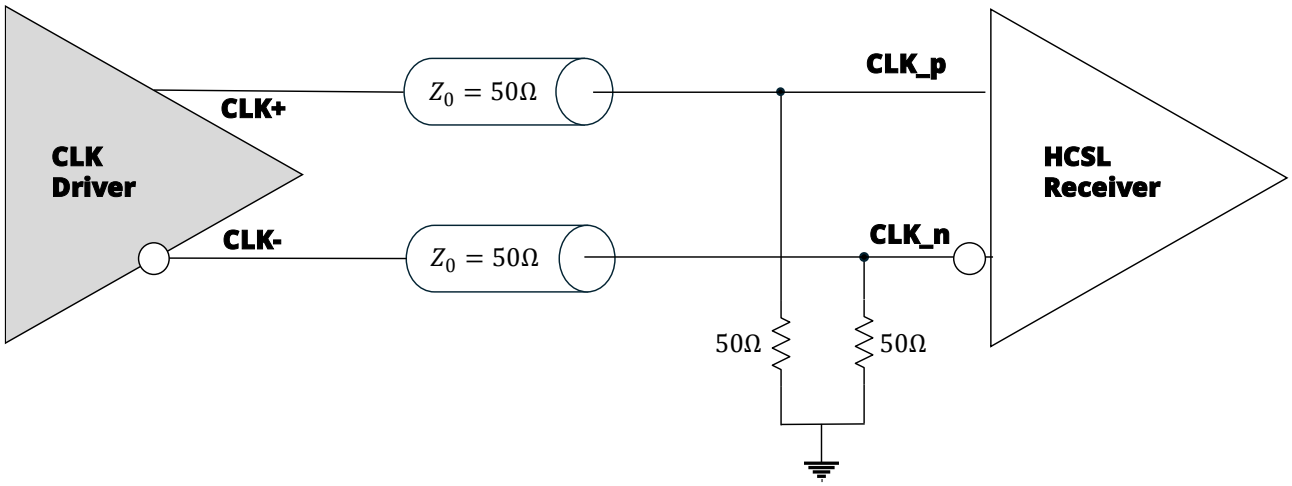


Figure 15. HCSL Output Driver with 50 Ω Receiver Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL	1.35V	DC	50 Ω to GND

Output Timing

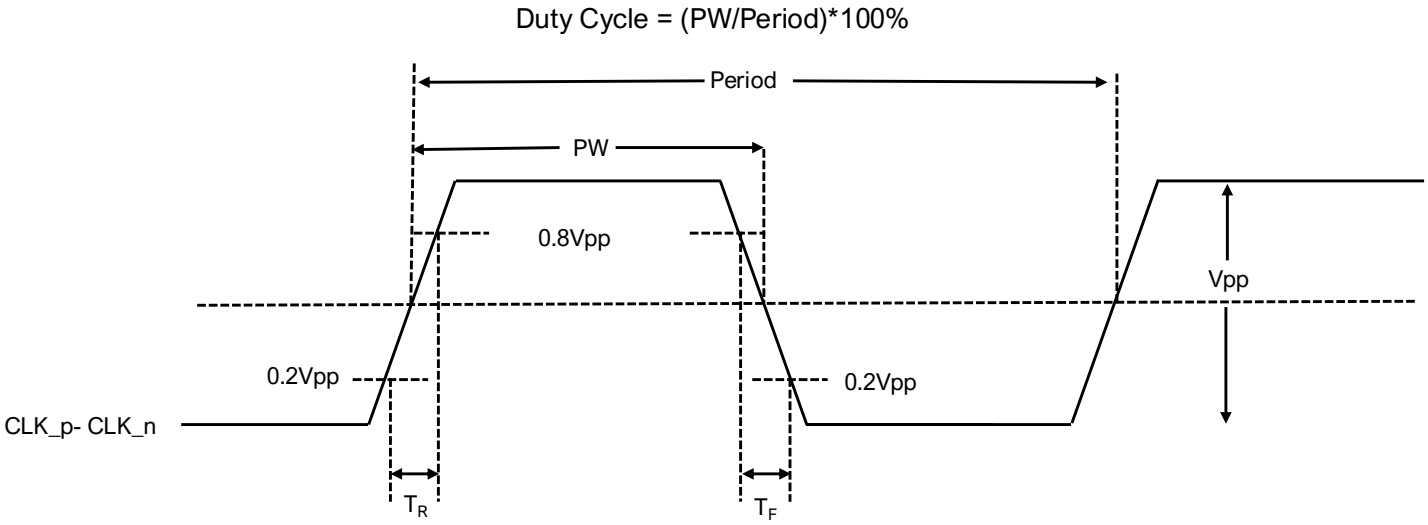


Figure 16. Output Timing across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps

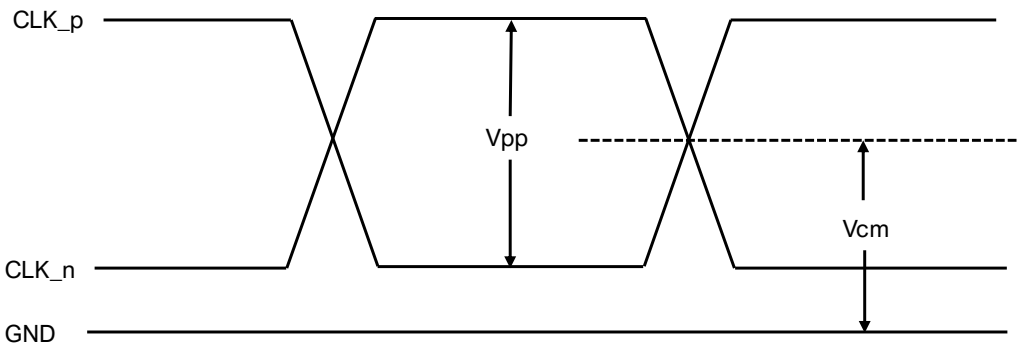


Figure 17. HCSL Output Level across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV

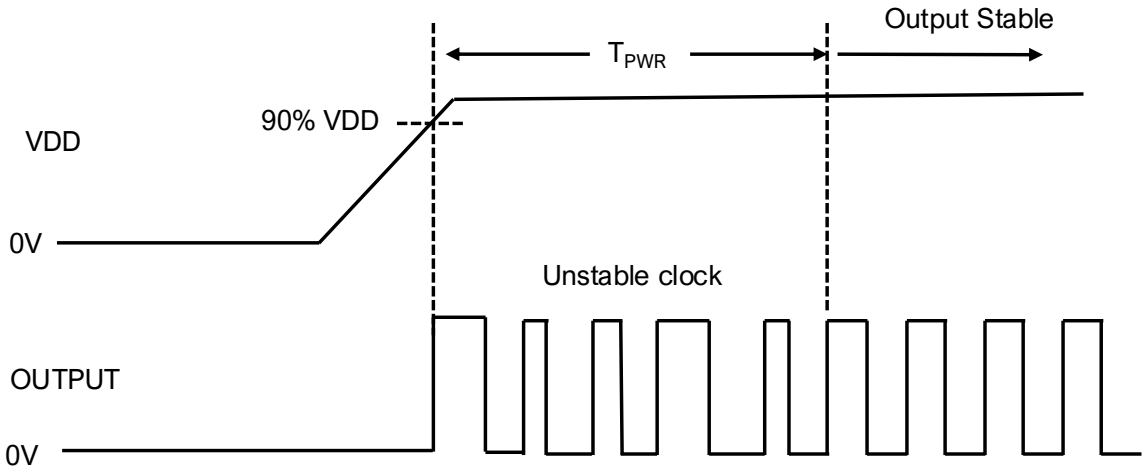


Figure 18. Powerup Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

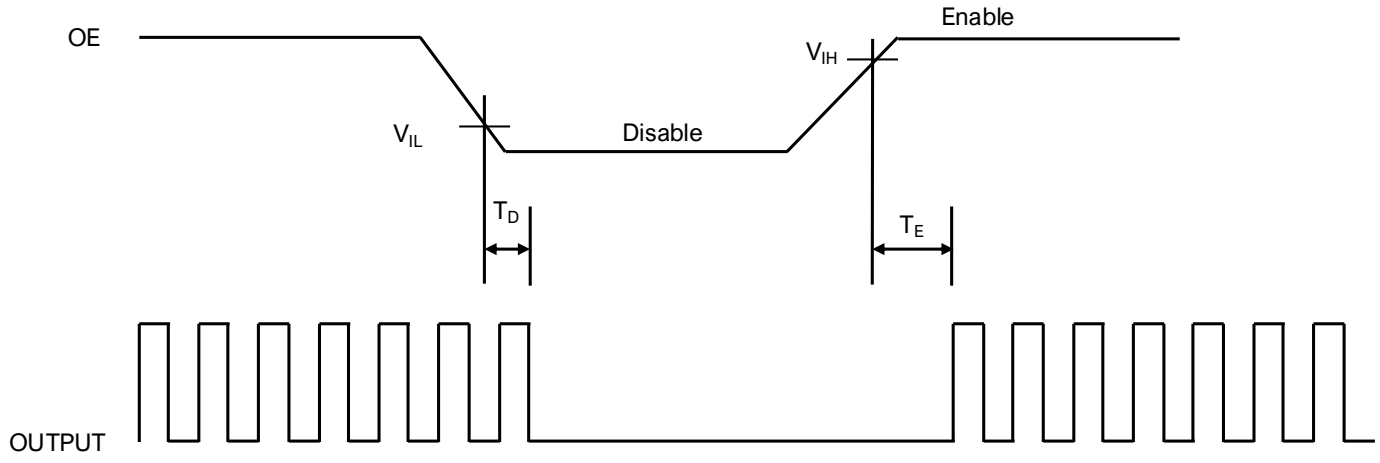


Figure 19. OE Enable/Disable Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs

Packaging Information

Figure 20 shows the MS1153 packaging drawing

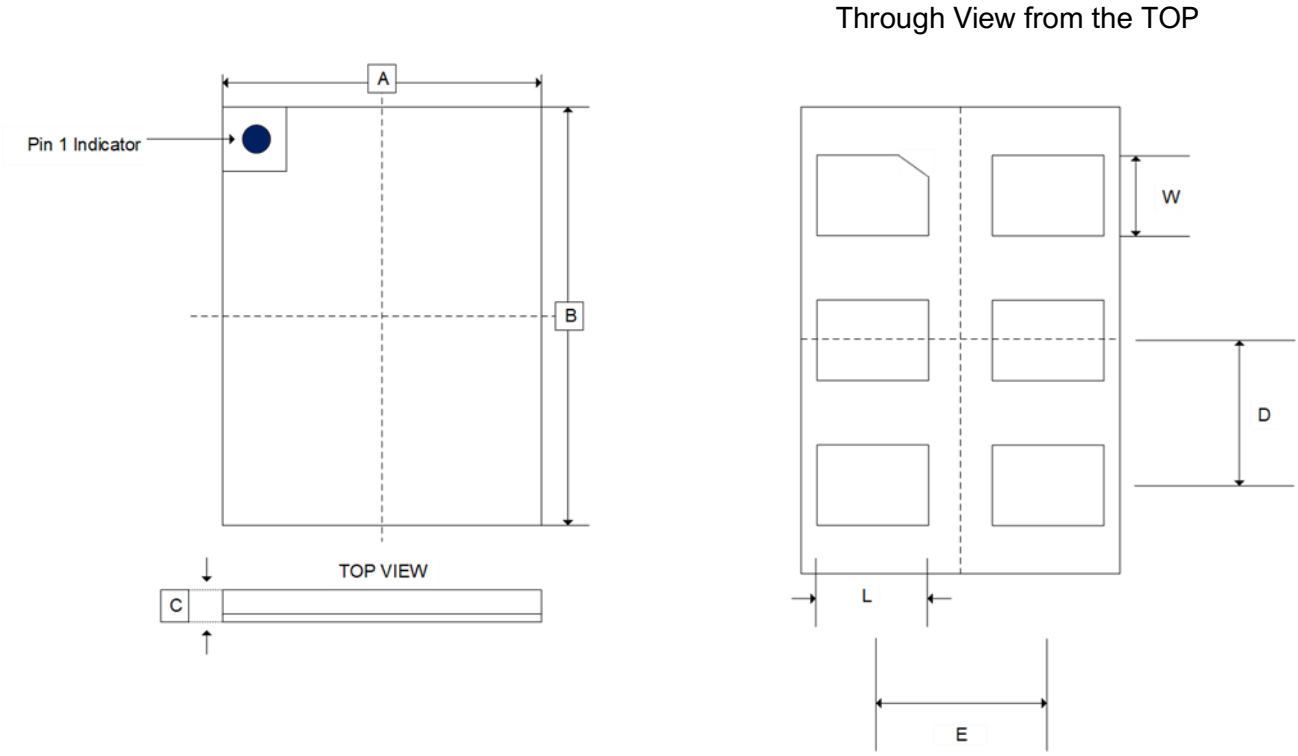


Figure 20. MS1153 Packaging Drawing (2.5X2.0 mm)

Table 9. MS1153 Packaging Dimensions

Dimensions	Min	Nom	Max
A		2.00 BSC	
B		2.50 BSC	
C	0.86	0.96	1.06
L	0.55	0.60	0.65
W	0.35	0.40	0.45
D		0.85 BSC	
E		1 BSC	
Package Edge Tolerance		0.1	
Mold Flatness		0.2	
Coplanarity		0.08	

Note: All dimensions are in millimeters

Packaging Land Pattern

Figure 21 shows the MS1153 PCB land pattern.
Note: All dimensions are in millimeters

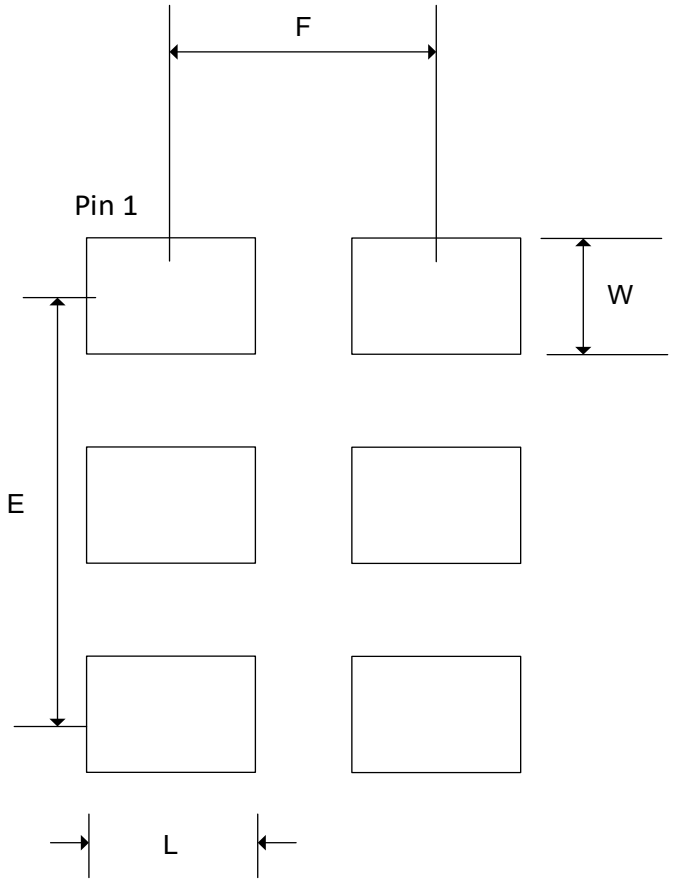


Figure 21. MS1153 Packaging Land Pattern Drawing (2.5X2.0 mm)

Table 10. MS1153 Packaging Land Pattern Dimensions

Dimensions	Length
L	0.75
W	0.55
E	1.7
F	1

Packaging Information

Figure 22 shows the MS1193 packaging drawing

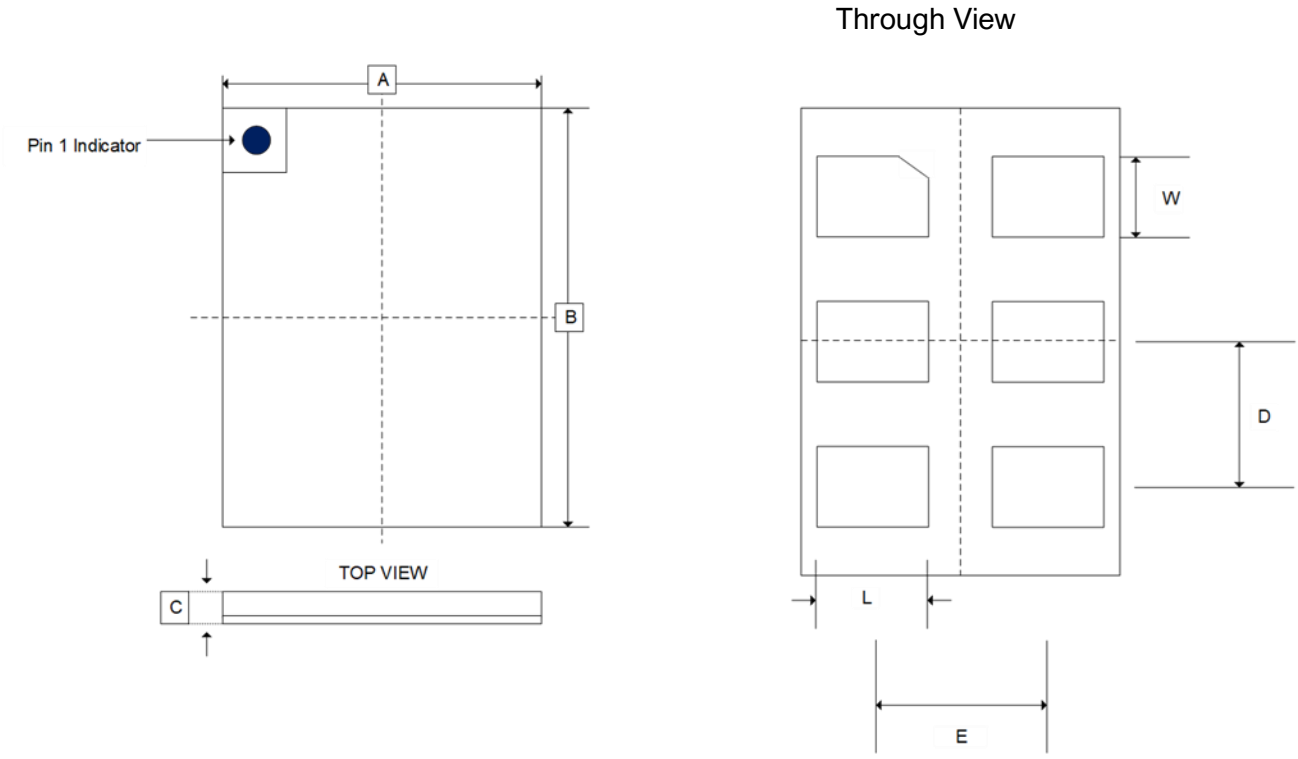


Figure 22. MS1193 Packaging Drawing (2.0X1.6 mm)

Table 11. MS1193 Packaging Dimensions

Dimensions	Min	Nom	Max
A		1.6 BSC	
B		2.0 BSC	
C	1.246	1.346	1.446
L	0.45	0.5	0.55
W	0.30	0.35	0.40
D		0.75 BSC	
E		0.95 BSC	
Package Edge Tolerance		0.1	
Mold Flatness		0.1	
Coplanarity		0.08	

Note: All dimensions are in millimeters

Packaging Land Pattern

Figure 22 shows the MMS1193 PCB land pattern.
Note: All dimensions are in millimeters

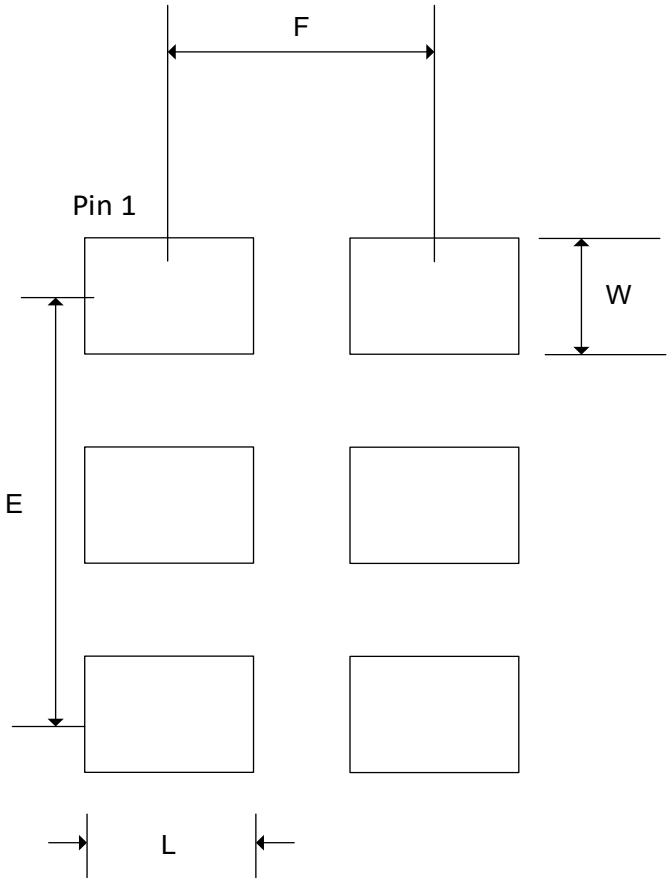


Figure 23. MS1193 Packaging Land Pattern Drawing (2.0X1.6 mm)

Table 12. MS1193 Packaging Land Pattern Dimensions

Dimensions	Length
L	0.80
W	0.524
E	1.564
F	1.15

Note: All dimensions are in millimeters

Device Top Marking

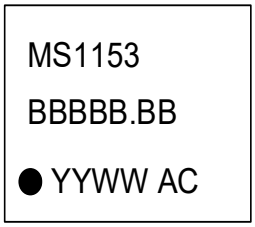


Figure 24. MS1153 Device Top Marking Showing Pin 1

Table 13. MS1153 Device Marking Legend

Line	Position	Description
1	1	Product Marking
2	1-5	Lot Number
	6-7	Wafer Number
3	Lot Trace Code	
	1	Pin 1 Orientation Mark (Dot)
	2-3	Year (last two digits of the year)
	4-5	Calendar Work Week Number (1-53)
	7-8	Assembly Code

Device Top Marking

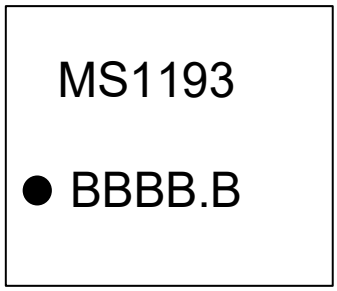


Figure 25. MS1193 Device Top Marking Showing Pin 1

Table 14. MS1193 Device Marking Legend

Line	Position	Description
1	1	Product Marking
2	1	Pin 1 Orientation Mark (Dot)
	2-5	Lot Number
	6	Wafer Number

Reflow Profile (IPC/JEDEC-STD-020)

Figure 26 shows the reflow profile for MS1153/MS1193

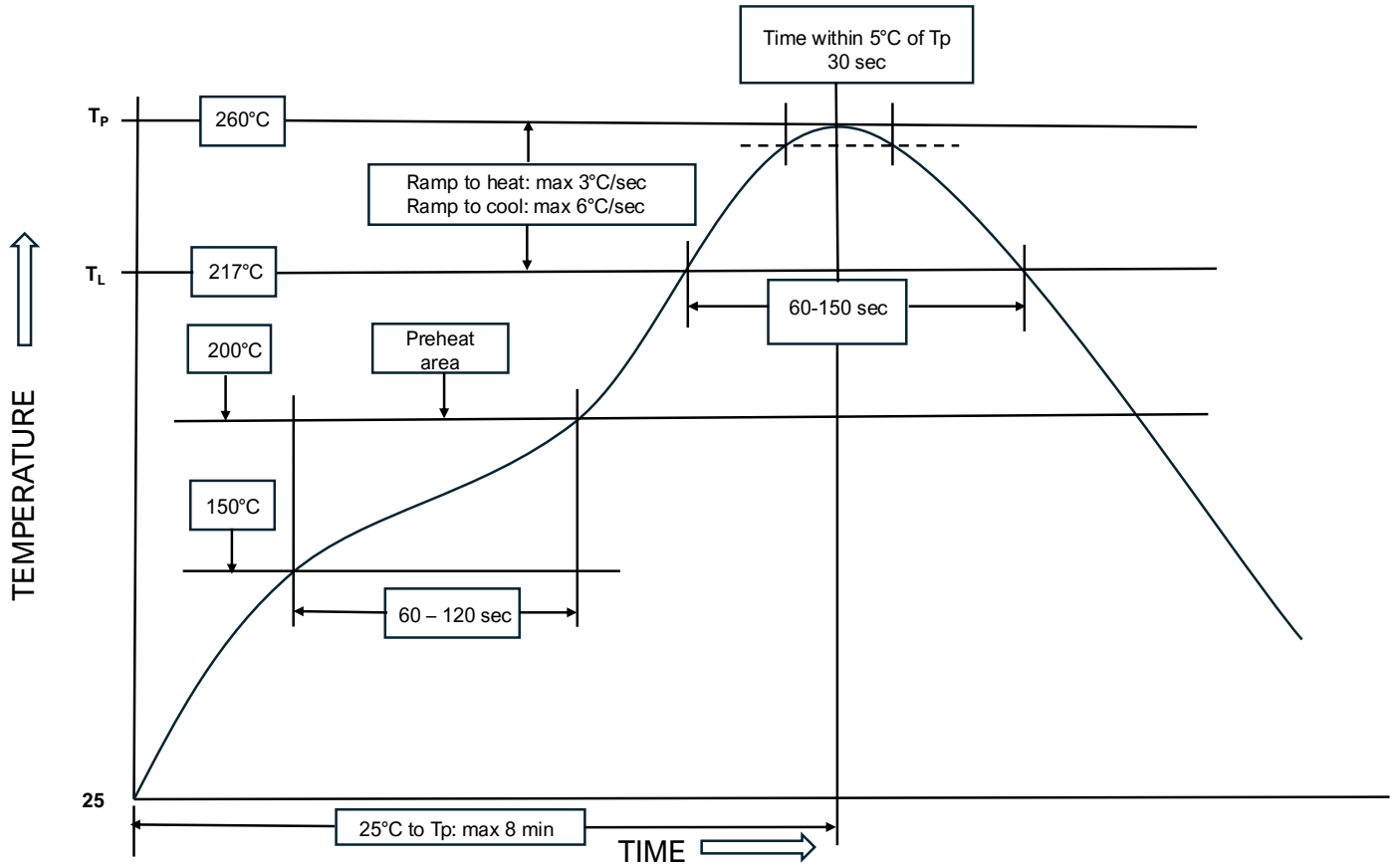


Figure 26. MS1153/MS1193 Reflow Profile

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