Ultra Low Additive Jitter Differential Clock Buffer (1:8)

Features

- Low additive jitter
  - 8 fs at 2 GHz
  - 16 fs at 312.5 MHz
  - 25 fs at 156.25 MHz
- Eight programmable outputs
- Programmable individual integer dividers
  - Divider range: 1 to 64
- Output frequency range:
  - Up to 2.5 GHz
- Output Formats: CML/LVDS/LVDS-EXT/LVPECL/HCSL
- Factory programmable NVM memory
- Asynchronous OE control
- Low Output-Output Skew: 10 ps
- Single 1.8V supply
- Temperature range of -40°C to 85°C
- Temperature range of -40°C to 105°C
- 5x5mm 32LGA Package

Applications

- Wired and Wireless Communications
- Switches, Routers, and Optical Networks
- Backplanes
- 5G and 6G massive MIMO radio Systems and Base-stations
- Datacenters' Servers, Acceleration and Storage
- Industrial and Medical applications
- Low jitter clock trees
- General purpose clock distribution

General Description

The MS2700 is an ultra-low jitter Distribution buffer that is ideal for clock distribution and redundant clocking applications. The MS2700 features additive jitter of 8 fs and operates over a wide frequency range from 100 MHz to 2.5 GHz.

MS2700 features eight output buffers with individual integer dividers that can be programmed to produce any frequencies from DC to 2.5 GHz.

The product can be factory programmed using non-volatile memory (NVM). This pre-programmed factory setting will be the power up condition of the device at for the frequencies and output interface.

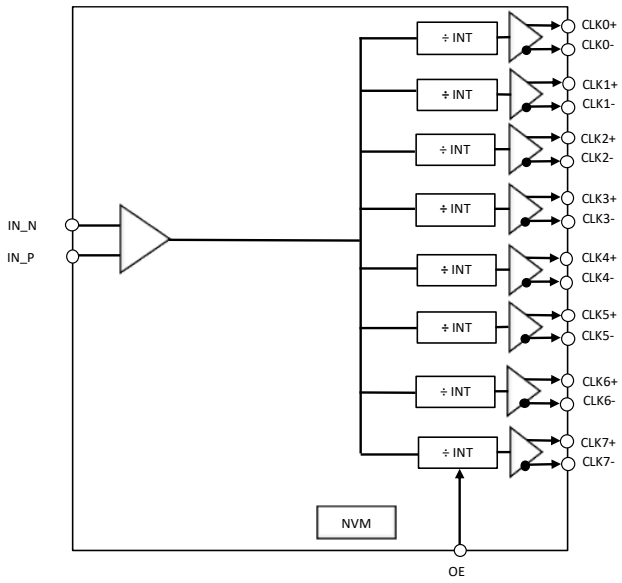

Figure 1. Functional Block Diagram

Pin Assignment and Pin Descriptions

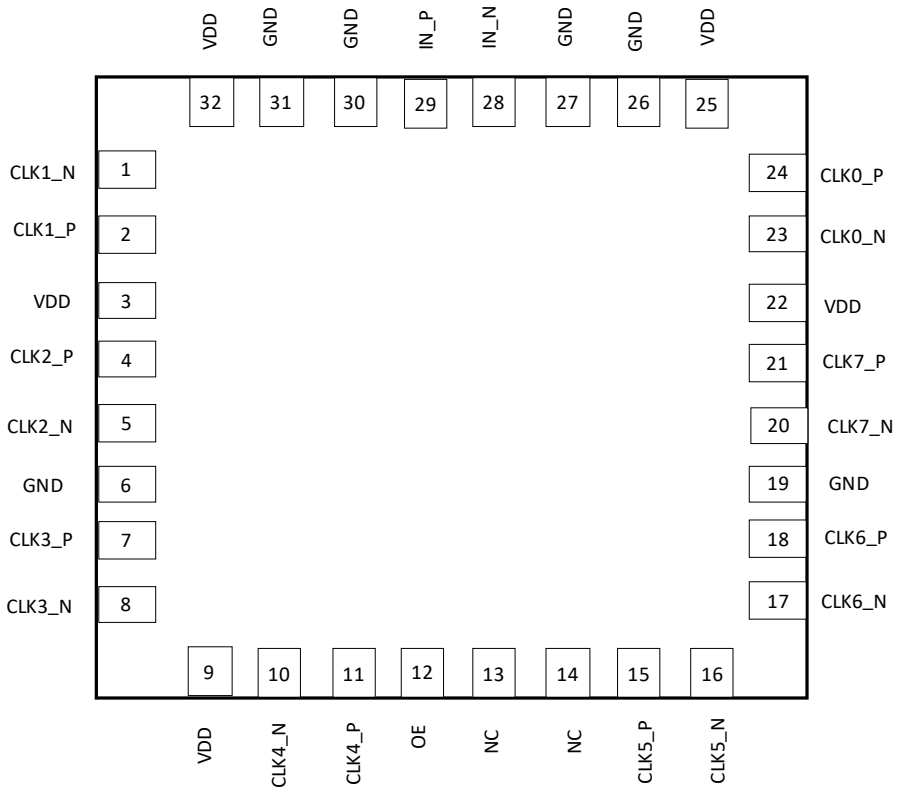

Figure 2. MS2700 Pin Assignment

Table 1. MS2700 Pin Descriptions

Pin No.	Name	I/O	Description
1	CLK1_N	O	Differential Clock Output
2	CLK1_P		
4	CLK2_P	O	Differential Clock Output
5	CLK2_N		
7	CLK3_P	O	Differential Clock Output
8	CLK3_N		
10	CLK4_N	O	Differential Clock Output
11	CLK4_P		
12	OE	I	Output Enable
15	CLK5_P	O	Differential Clock Output
16	CLK5_N		
17	CLK6_N	O	Differential Clock Output
18	CLK6_P		
20	CLK7_N	O	Differential Clock Output
21	CLK7_P		
23	CLK0_N	O	Differential Clock Output
24	CLK0_P		
28	IN_N	I	Differential Clock Input
29	IN_P		
13,14	NC		No Connect
3,9,22,25,32	VDD	P	1.8V Supply
6,19,26,27,30,31	GND	P	Ground

Part Ordering Information

Figure 3 shows a logic tree for ordering each of the available parts.

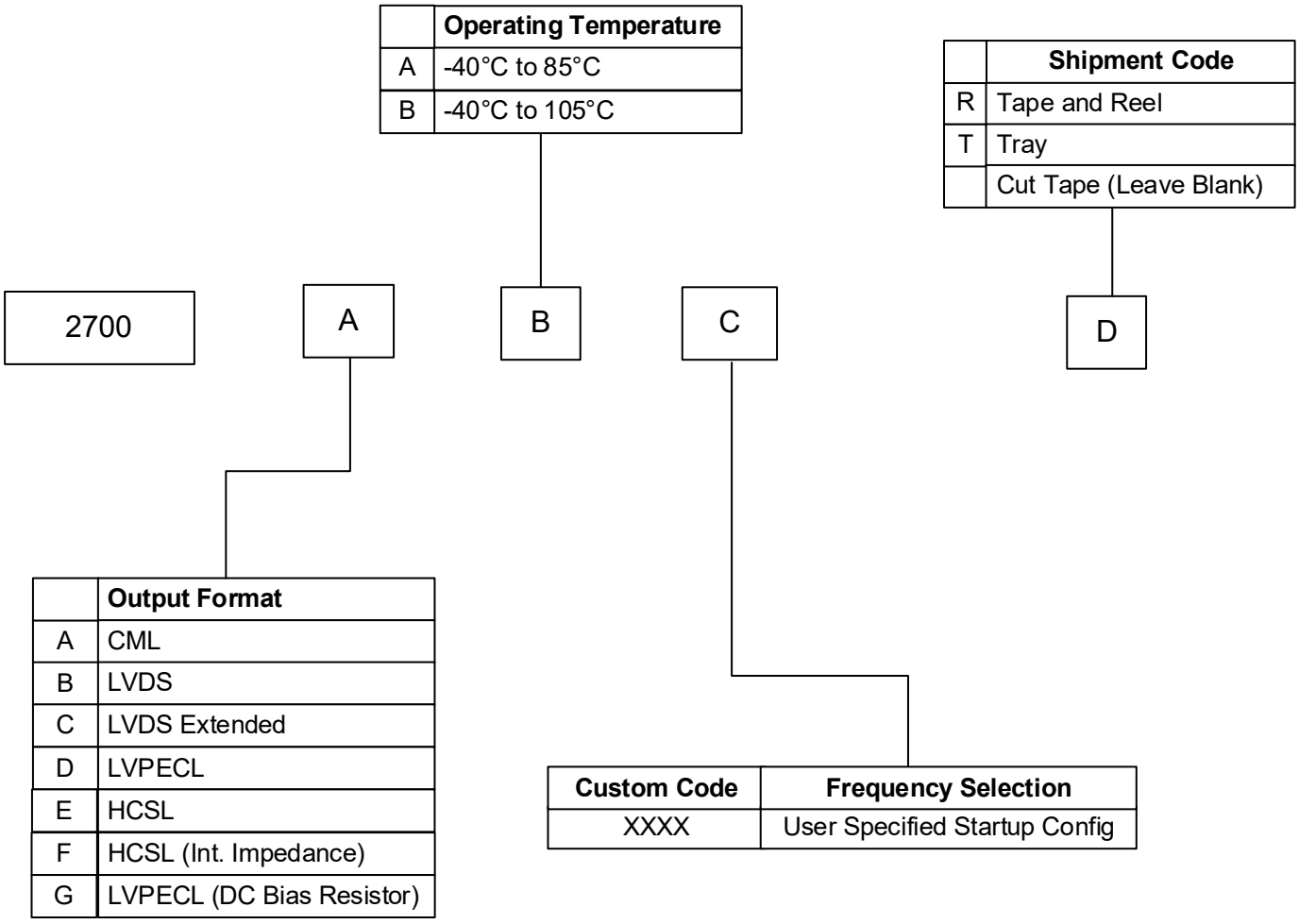

Figure 3. MS2700 Part Ordering Information

Table 2. Example of ordering part number

Base P/N	Output Format	Operating Temperature	Divider Setting	Custom Code	Shipment Type	**Ordering part number**
2700	LVDS	-40C to 85C	Divide by 2	0002*	Tape and Reel	**2700BA0002R**
2700	HCSL	-40C to 105C	Divide by 1	0001*	Tape and Reel	**2700EB0001R**

* Frequency Code table will be provided by factory based on customer requirements

Specifications

Table 3. Electrical Specifications
Typical values are specified at T_A= 25°C, V_{DD}=1.8V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard termination. A 0.1uF and 10uf bypass capacitor should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Frequency Range						
Input Frequency Range	F_{IN}		100		2500	MHz
Differential Input Swing	V_{IN}	Vpk-pk (AC-Coupled)	0.2		1.8	V
Output Frequency Range	F_{OUT}		100		2500	MHz
Additive Jitter Characteristics						
RMS Phase Jitter (12 KHz – 20 MHz)	Φ_{JITTER}	F_{OUT}= 2 GHz		8	12	fs
		F_{OUT}=312.5 MHz		16	22	
		F_{OUT}=156.25 MHz		25	35	
Note: Phase jitter measured on Agilent 5052B Signal Source Analyzer						
Operating Voltage/Temperature Range						
Supply Voltage	V_{DD}		1.71 -5%	1.8	1.89 +5%	V
Temperature Range	T_A	Industrial Temperature	-40		85	°C
		Extended Industrial Temperature	-40		105	°C

Current Consumption

Supply Current (Excluding Output)	I_{DD}	IDD		10		mA
Per-Output Buffer Supply Current	I_{DDOX}	LVDS Output		4		mA
		LVDS-EXT Output		6		mA
		All Other Outputs		14		mA

Input Characteristics

Digital Input Levels(OE)	V_{IH}		$0.7XV_{DD}$			V
	V_{IL}				$0.3XV_{DD}$	V
Input Capacitance	C_{IN}			1.5		pF
Input Resistance	R_{IN}			20		kΩ
Output Enable (OE)	T_D	Output Disable Time			3	us
	T_E	Output Enable Time			20	us
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms
Output Lock Time	T_{LOCK}	Time from input signal to a stable output	10			us
Propagation Delay	T_{PD}	Input cross point to output cross point			1	ns

PSRR Characteristics

Power Supply-Induced Phase Noise	PSPN	Spurs induced by 50mV power supply ripples (312.5MHz)		-114		dBc
Power Supply-Jitter Sensitivity	PSJS			0.1		fs/mv

Note:

(1) Measured with 50 mVpp ripple from 50 KHz to 1 MHz applied on VDD Pin

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps
CML Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 5, Figure 6	0.6	0.8	1	V
LVDS Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 7	0.5	0.7	0.9	V
LVDS-EXT Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 7	0.8	1.2	1.6	V
LVPECL Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 8, Figure 9	1.2	1.4	1.6	V
HCSL Output (AC or DC-Coupled)	Vpp	Differential Pk-Pk See Figure 10, Figure 11	1.1	1.35	1.6	V
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV
Output-Output Crosstalk	XTALK	Measure spur from adjacent output		-75		dBc
Output-Output Skew	Tsk			10		ps

Unless otherwise specified, all differential output amplitudes are measured across a 100 Ω differential load or the termination network shown in the referenced output driver figures on the following pages

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O (OE)	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Junction Temperature		150	°C
Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.			

Table 5. Environmental Compliance

Parameter	Test Condition	Value	Unit
Moisture Sensitivity Level (MSL)	MSL3 @260°C		
Soldering Temperature	MIL-STD-883, Method 2003	260	°C
Electrostatic Discharge (HBM)	JEDEC JS-001	2000	V
Charge-Device Model (CDM)	JEDEC JESD22-C101	500	V
Latch-up Compliance	JESD78 Compliant		

Table 6. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
5mm x 5mm 32 pin LGA	Maximum Board Temperature	T_B	125	°C
	Thermal Resistance, Junction to Ambient	$ø_{JA}$	50	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	34	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C
Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.				

Output Terminations

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff
LVDS	0.7V	AC	100 Ω diff
LVDS-EXT	1.2V	AC	100 Ω diff
LVPECL	1.4V	AC	50 Ω to VT
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT
HCSL (Int Term)	1.35V	AC or DC	None
HCSL	1.35V	DC	50 Ω to GND

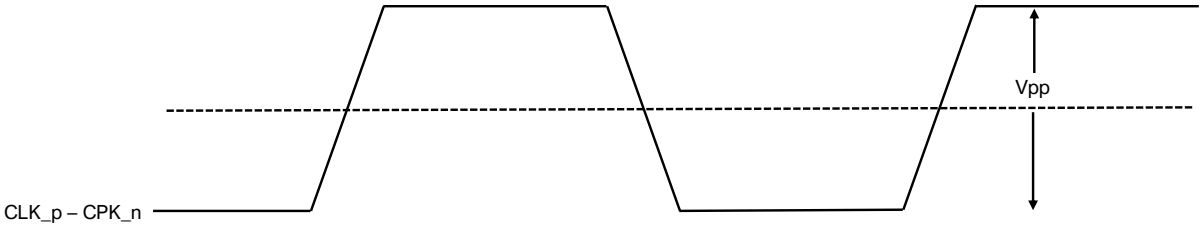

Figure 4. Differential Output Swing

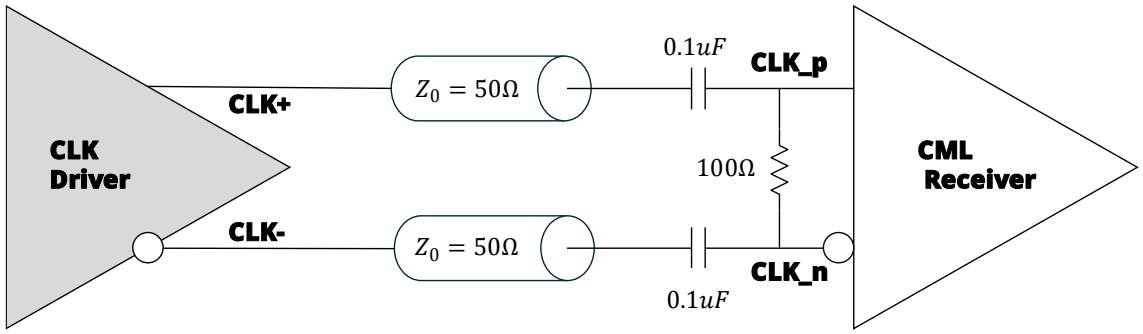

Figure 5. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

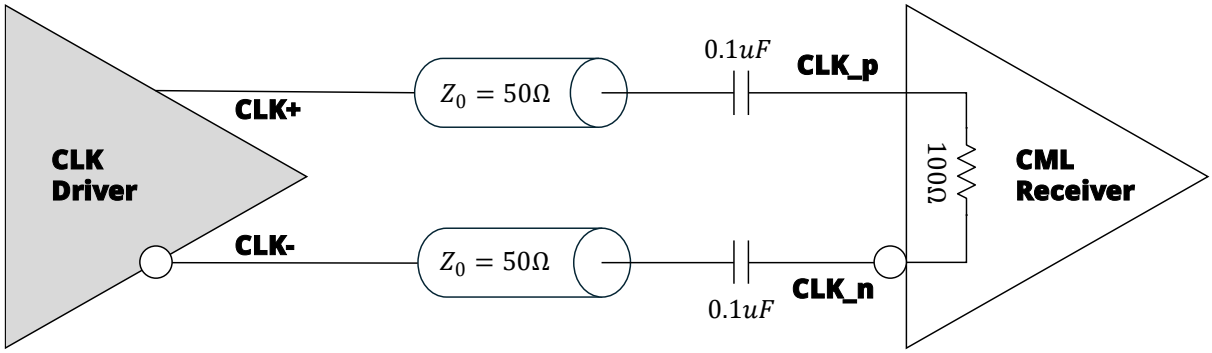

Figure 6. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

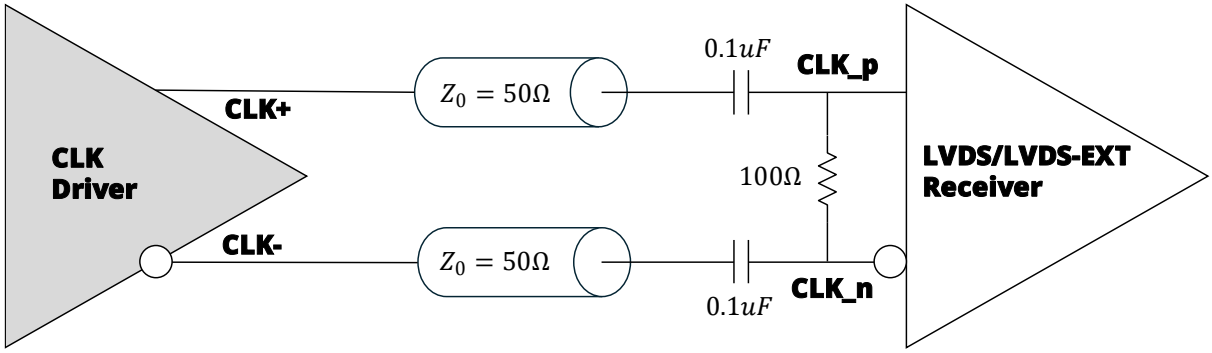

Figure 7. LVDS/LVDS-EXT Output Driver with 100 Ω Differential Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVDS/LVDS-EXT	0.7V/1.2V	AC	100 Ω diff

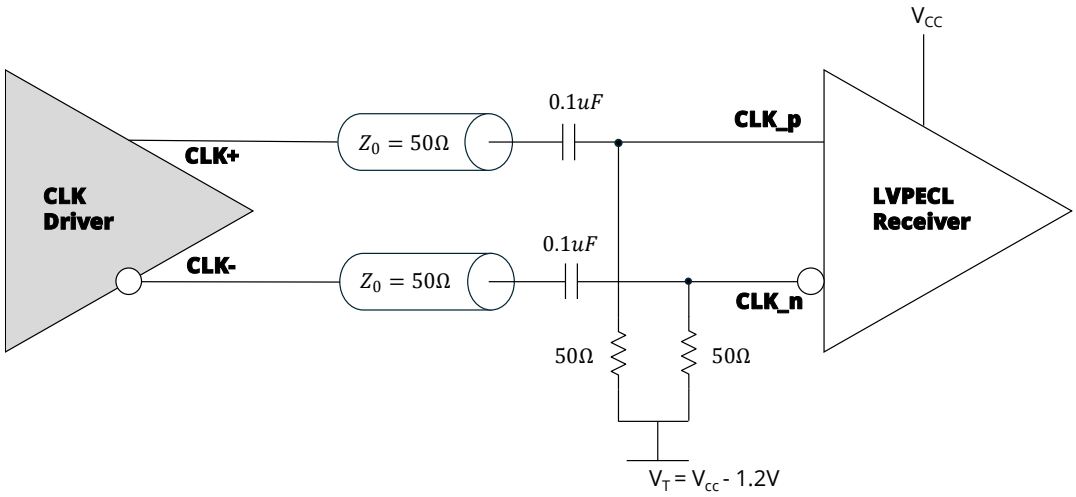

Figure 8. LVPECL Output Driver with External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL	1.4V	AC	50Ω to VT

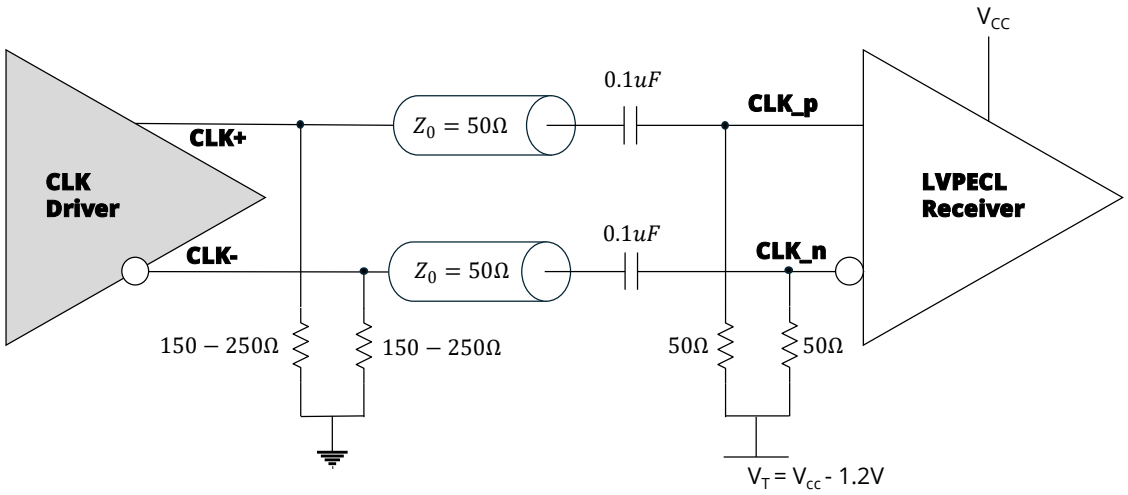

Figure 9. LVPECL Output Driver with Source Bias Resistors and External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT

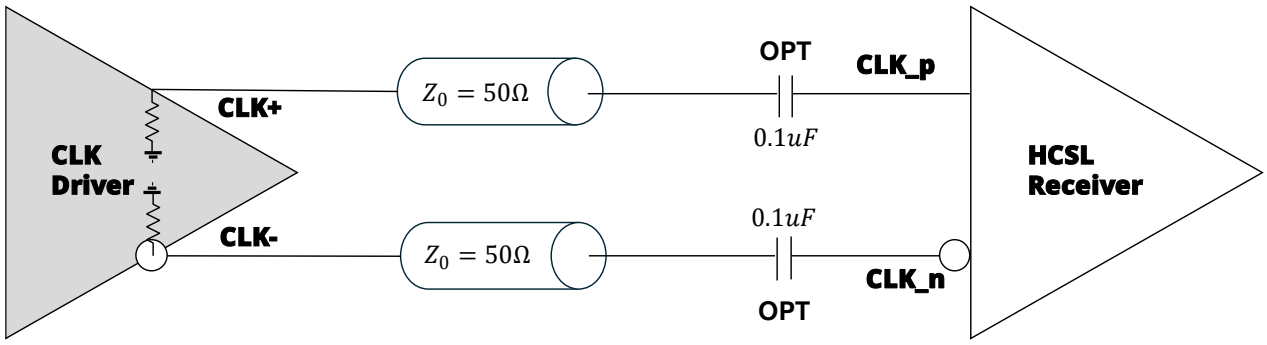

Figure 10. HCSL Output Driver with Integrated Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL (Int Term)	1.35V	AC/DC	None

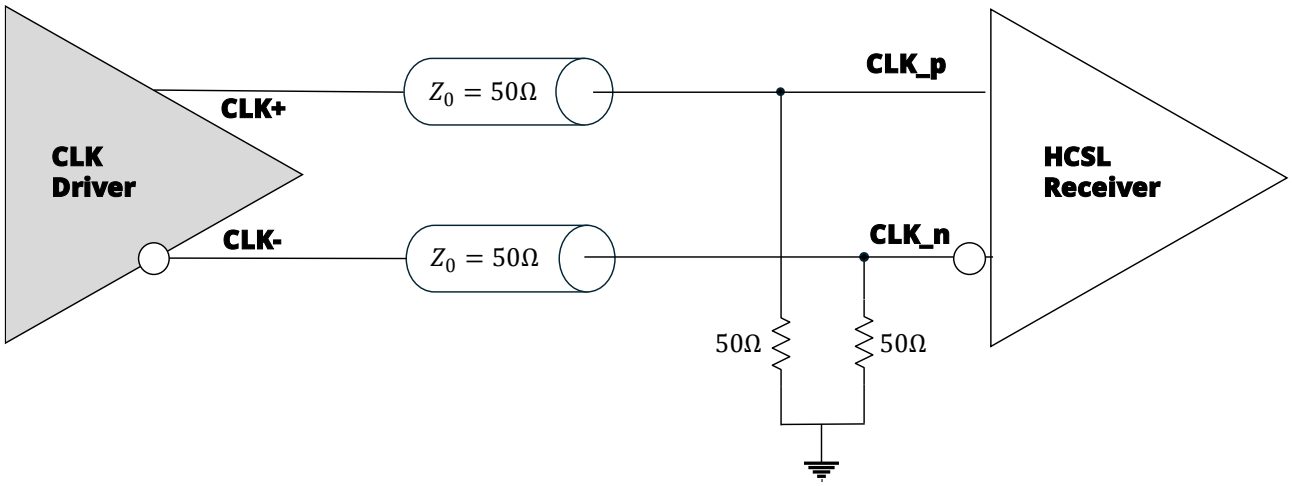

Figure 11. HCSL Output Driver with 50 Ω Receiver Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL	1.35V	DC	50 Ω to GND

Output Timing

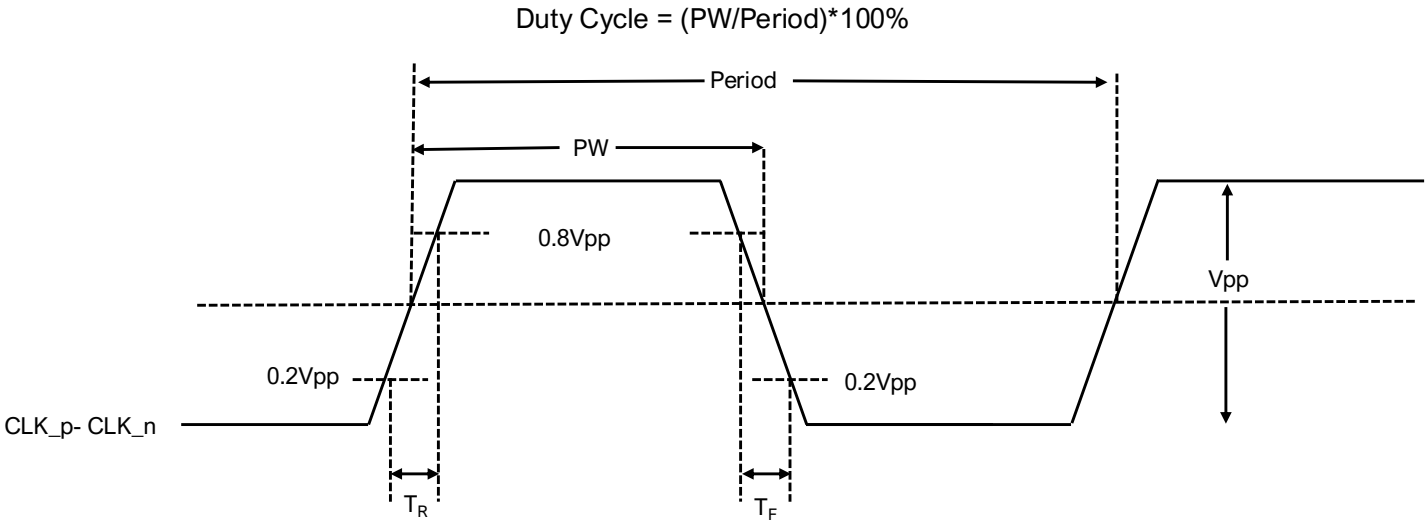

Figure 12. Output Timing across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps

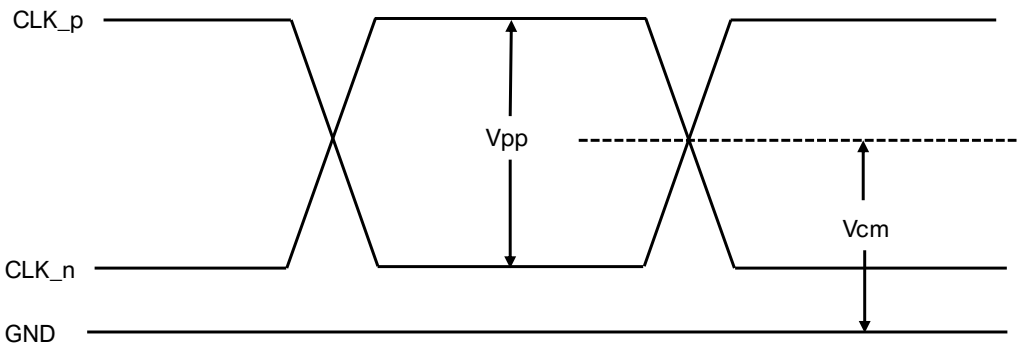

Figure 13. HCSL Output Level across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV

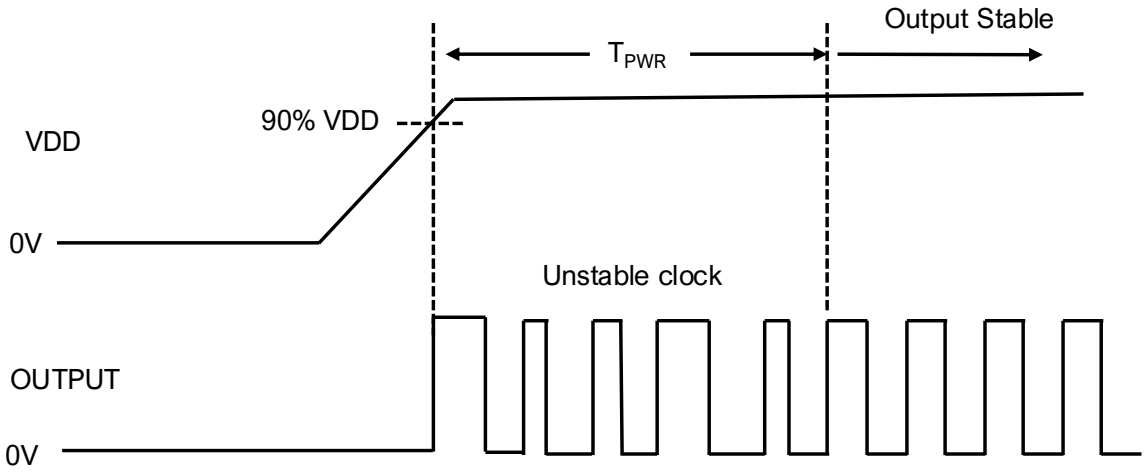

Figure 14. Powerup Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

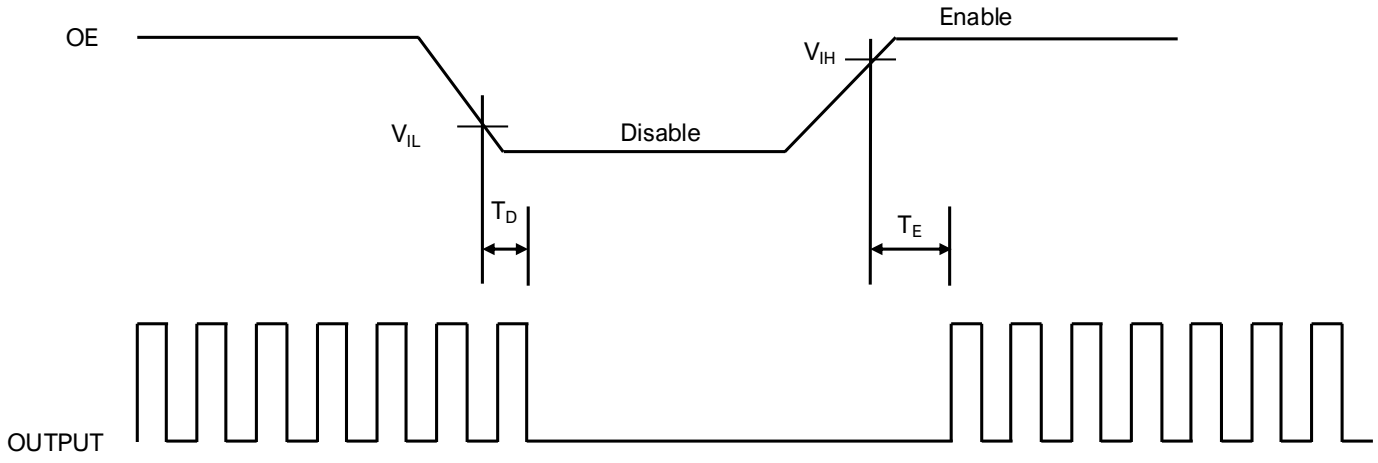

Figure 15. OE Enable/Disable Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs

Packaging Information

Figure 16 shows the MS2700 packaging drawing

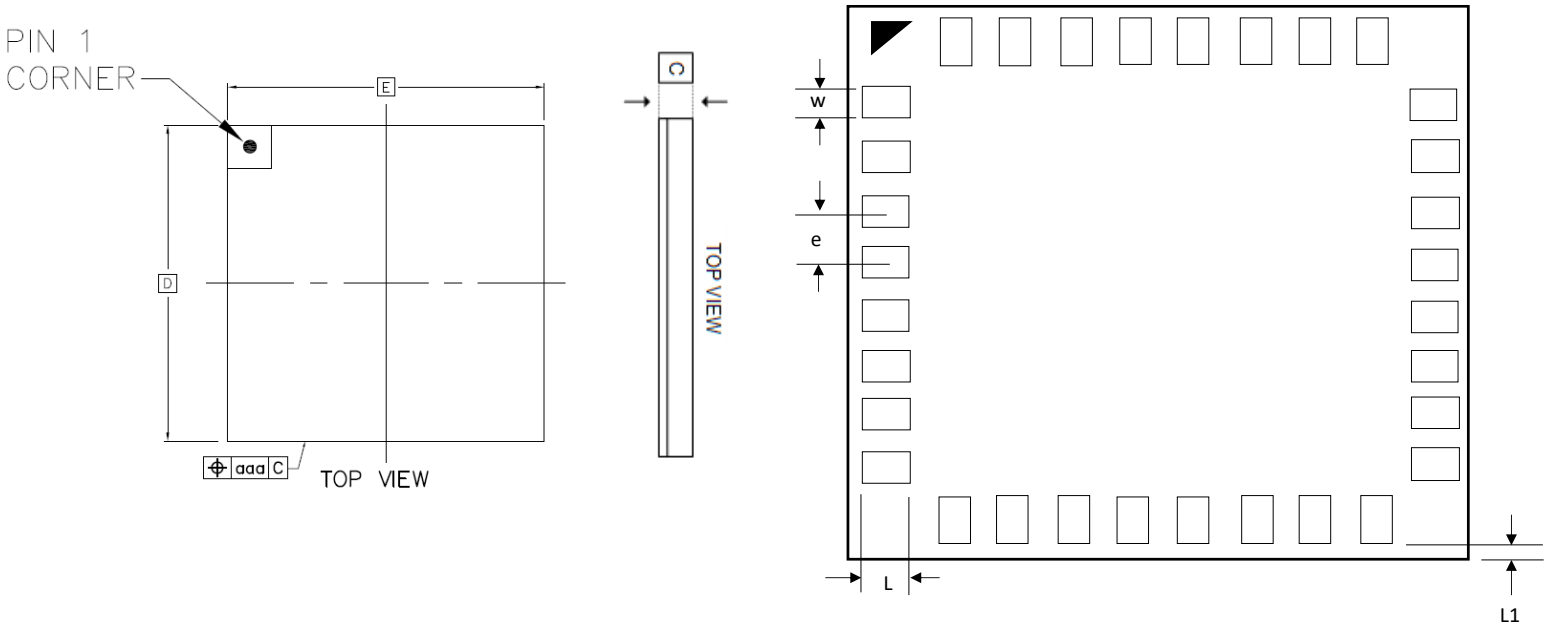

Figure 16. MS2700 Packaging Drawing (5mm x 5 mm,)

Table 7. MS2700 Packaging Dimensions

Dimensions	Min	Nom	Max
C	0.903	0.96	1.1
D		5 BSC	
E		5 BSC	
L	0.35	0.4	045
W	0.20	0.25	0.30
L1	0.05	0.10	0.15
e		0.5 BSC	
Package Edge Tolerance		0.1	
Mold Flatness		0.1	
Coplanarity		0.08	

Note: All dimensions are in millimeters

Packaging Land Pattern

Figure 17 shows the MS2700 PCB land pattern.

Note: All dimensions are in millimeters

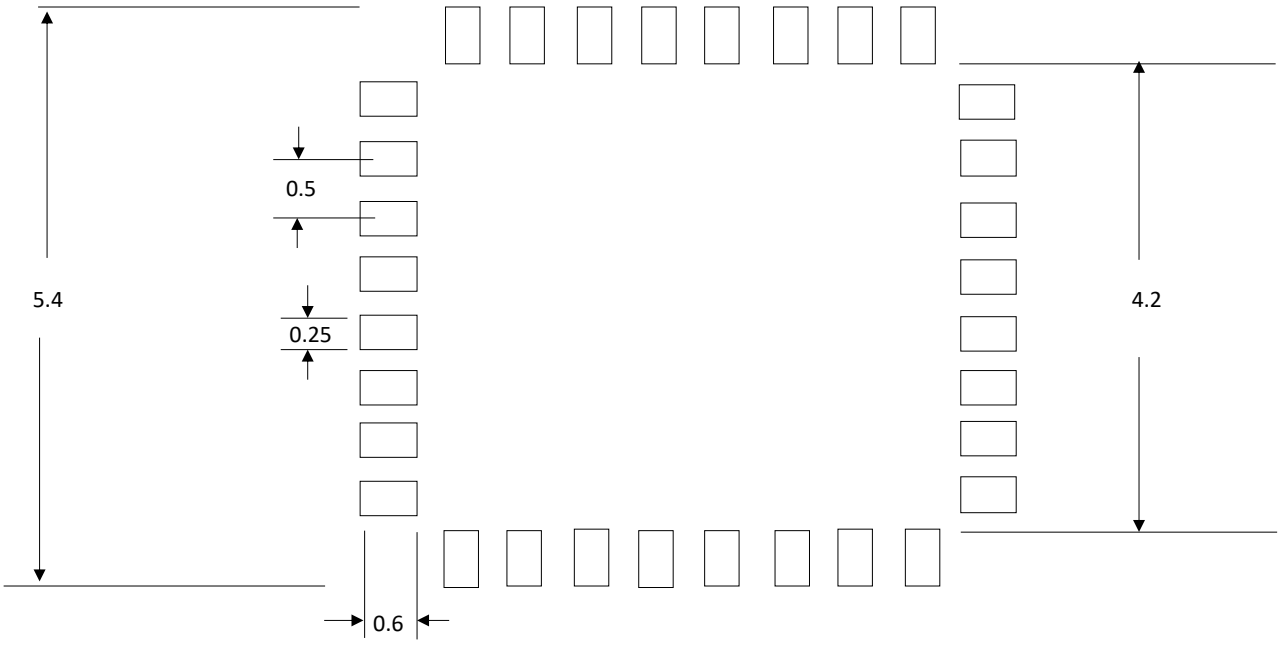

Figure 17. MS2700 Packaging Land Pattern Drawing (5X5 mm)

Device Top Marking

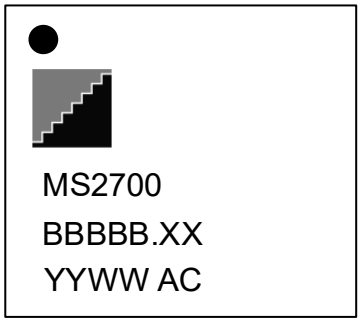

Figure 18. MS2700 Device Top Marking Showing Pin 1

Table 8. MS2700 Device Marking Legend

Line	Position	Description
1	1	Pin 1 Orientation Mark (Dot)
2	1	Mixed-Signal Logo
3	1-6	Product Marking
4	1-5	Wafer Lot Number
	6-7	Wafer #
5	Lot Trace Code	
	1-2	Year (last two digits of the year)
	3-4	Calendar Work Week Number (1-53)
	5-6	Assembly Code

Reflow Profile (IPC/JEDEC-STD-020)

Figure 19 shows the reflow profile for MS2700

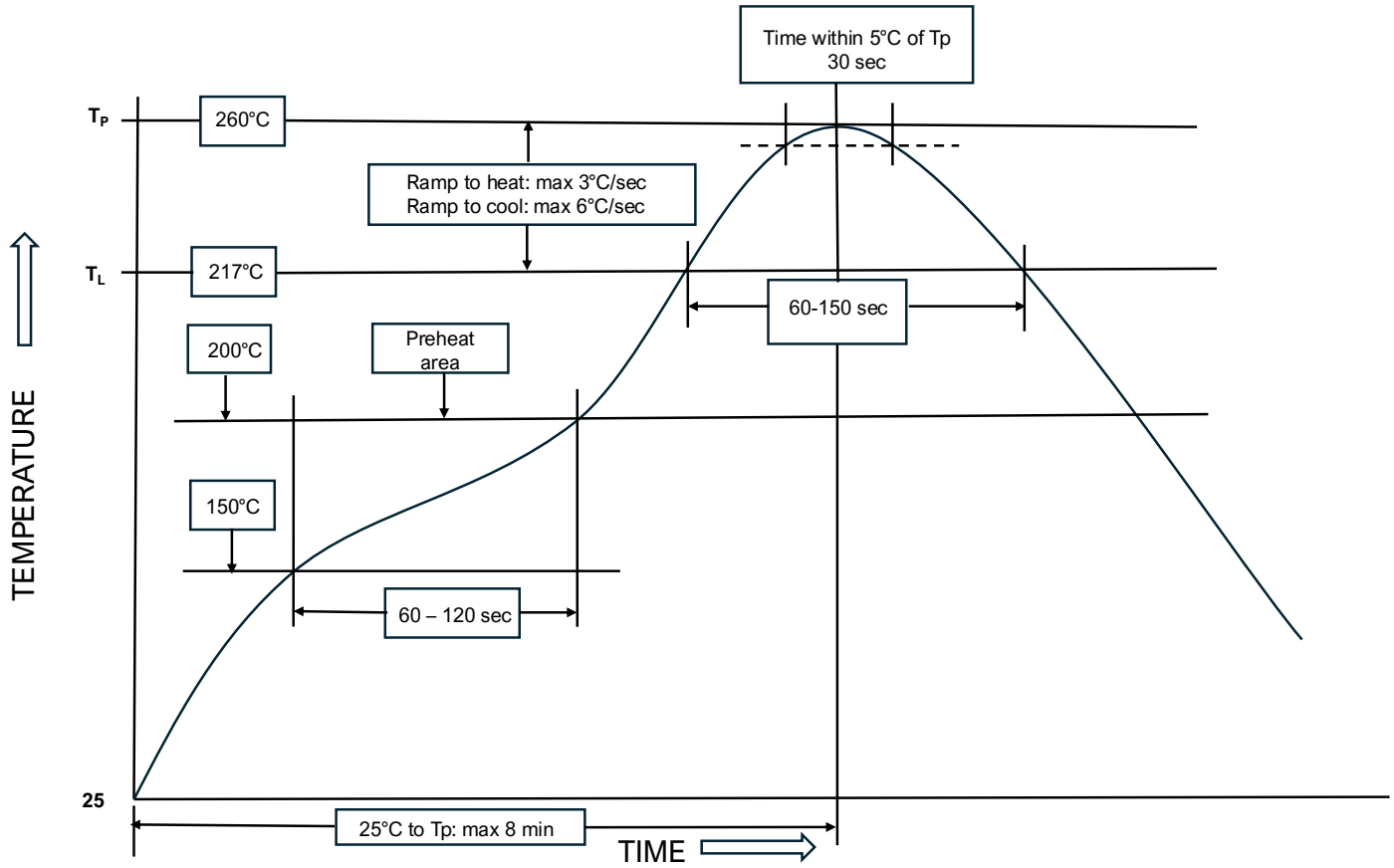

Figure 19. MS2700 Reflow Profile

IMPORTANT NOTICE AND DISCLAIMER

MIXED-SIGNAL DEVICES INC. PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

Mailing Address: Mixed-Signal Devices Inc, 2 Venture, Suite 300, Irvine, California 92618, USA