

High-Performance 2-42 GHz CW and FMCW Chirp Generator for Radar Systems

FEATURES

- Superior phase noise of -142 dBc/Hz at 1 MHz offset for 2 GHz carrier frequency
- Excellent linearity: < 0.002% Peak INL
- Wide chirp bandwidth up to 4 GHz
- Ultra-low jitter at 30 fs (12 kHz to 20 MHz integration bandwidth)
- Fully configurable chirp parameters, symmetrical and asymmetrical: sawtooth± and triangle± programmable start and stop frequencies
- Advanced chirp signatures such as frequency hopping, pulse phase modulation, etc.
- Output Frequency Range
Differential: S-band, C-band, X-band, Ku-band K-band, Ka-band
- Input Reference Frequency Range
Differential: 1 MHz to 750 MHz
- Chirp synchronized by external SYNC signal or via I²C or SPI
- I²C and SPI programmable
- Single 1.8V supply with internal regulators
- Superior power supply noise immunity
- Operating Temperature Range: -40°C to 85°C
- Industry standard 6x6 mm 60-pin BGA package
- Robust ESD protection: HBM 1000V, CDM 250V
- Lead free / RoHS compliant

APPLICATIONS

- High-Resolution Radar Systems
- Advanced Driver Assistance Systems (ADAS)
- Drone Altimeters and Navigation
- Robotics and Industrial Automation
- Gesture Recognition and Human Sensing
- Synthetic Aperture Radar and Imaging Systems
- Through-the-Wall and Ground Penetrating Radar (GPR)
- Security and Surveillance Radar
- Biosensing and Vital Sign Detection
- In-bed Patient Monitoring Systems
- Personal Health and Wellness Devices

GENERAL DESCRIPTION

The MS4000 is powered by our zeroDNL[®] technology, enabling perfectly spur-free multi-GS/s Digital-to-Analog Converters (DACs). It features significant advancements in Direct Digital Synthesis (DDS) and ultra-low phase noise clocks, delivering the industry's highest-linearity, fully programmable chirp waveforms with excellent close-in phase noise. Designed for demanding radar and sensing applications, the MS4000 supports frequency-hopped spread spectrum and precisely defined waveform profiles.

Field-programmable via I²C or SPI interfaces, the MS4000 provides flexibility and ease of integration. On-chip filtering and internal low-noise regulators ensure outstanding power supply noise rejection (PSRR), maintaining signal integrity even in challenging environments. The device also incorporates adaptive DSP algorithms that continuously monitor and optimize performance, delivering robust, consistent operation across process, voltage, and temperature (PVT) variations.

Functional Block Diagram

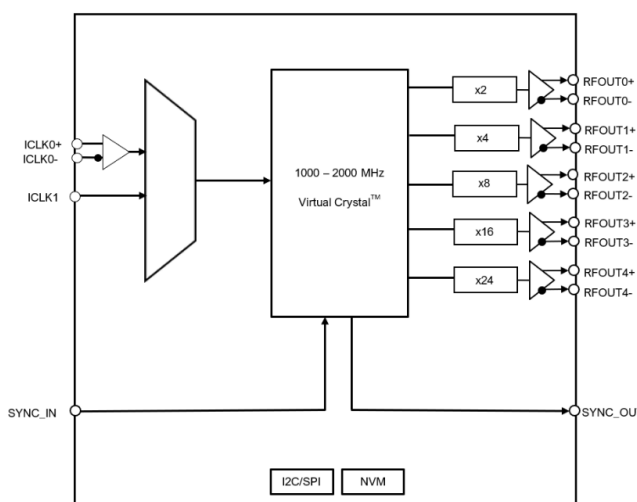


Figure. 1

SPECIFICATIONS

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage (1.8V)	-0.3	1.98	V
Digital I/O	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Soldering Temperature		260	°C
Junction Temperature		150	°C

Table 2. Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage	VDD	1.8V	1.71	1.8	1.89	V
Supply Current	IDD	1.8V		400		mA
Operating Temperature	Temp		-40°		85°	C

Table 3. Input Clock Specifications

VDD=1.8V +/-5%, Ta= Operating Temperature

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Units
Input Frequency Range	F _{in}	Differential	1		750	MHz
		Single-Ended			200	MHz
Input Voltage Swing	V _{in}	Differential AC-coupled	0.1		0.9	V _{pp} -SE
		Single-Ended	0.1		0.9	V _{pp} -SE
Input Resistance	R _{in}	Differential		16		kΩ
		Single-Ended		8		kΩ
Input Capacitance	C _{in}			2.4		pF
Slew Rate	SR		400			V/us

Table 4. RF Characteristics $V_{DD}=1.8V \pm 5\%$, T_a = Operating Temperature

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Units
Output Frequency Range	F_{OUT}					
RFOUT0	F_{OUT}		2		3.5	GHz
RFOUT1	F_{OUT}		3		7	GHz
RFOUT2	F_{OUT}		8		14	GHz
RFOUT3	F_{OUT}		24		27	GHz
RFOUT4	F_{OUT}		36		42	GHz
Output Power	P_O	Differential		-10		dBm
Output Return Loss, 3 GHz	R_L	Single-ended		-14		dB
Output Return Loss, 6 GHz	R_L	Single-ended		-13		dB
Output Return Loss, 12 GHz	R_L	Single-ended		-12		dB
Output Return Loss, 26 GHz	R_L	Single-ended		-11		dB
Output Return Loss, 40 GHz	R_L	Single-ended		-10		dB
Output Impedance	R_{OUT}	Differential		100		Ω

Table 5. Typical Output Phase Noise Characteristics $V_{DD}=1.8V$, $T_a= 25^\circ C$

Offset frequency	3 GHz	6 GHz	12 GHz	26 GHz	40 GHz	Unit
1 KHz	-81	-76	-69	-62	-60	dBc/Hz
10 KHz	-111	-105	-99	-92	-88	dBc/Hz
100 KHz	-133	-128	-121	-115	-110	dBc/Hz
1 MHz	-142	-137	-130	-123	-119	dBc/Hz
10 MHz	-142	-137	-130	-124	-120	dBc/Hz
20 MHz	-142	-137	-130	-124	-125	dBc/Hz
RMS Jitter (12-KHz – 20 MHz)	28	28	31	30	28	fs

Table 6. Typical Chirp Characteristics $V_{DD} = 1.8V$, $T_a = 25^{\circ}C$

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Units
Bandwidth, RFOUT0	$f_{BWR\text{FOUT}0}$				1	GHz
Bandwidth, RFOUT1	$f_{BWR\text{FOUT}1}$				2	GHz
Bandwidth, RFOUT2	$f_{BWR\text{FOUT}2}$				4	GHz
Bandwidth, RFOUT3	$f_{BWR\text{FOUT}3}$				5	GHz
Bandwidth, RFOUT4	$f_{BWR\text{FOUT}4}$				5	GHz
Ramp Rate	RR			300		MHz/ μ s
Linearity (RFOUT0-4) ¹	INL RMS			0.00006		
	INL Peak			0.0002		
	INL Avg			2×10^{-8}		

1 – Linearity is maintained across all frequencies from 2 – 42 GHz

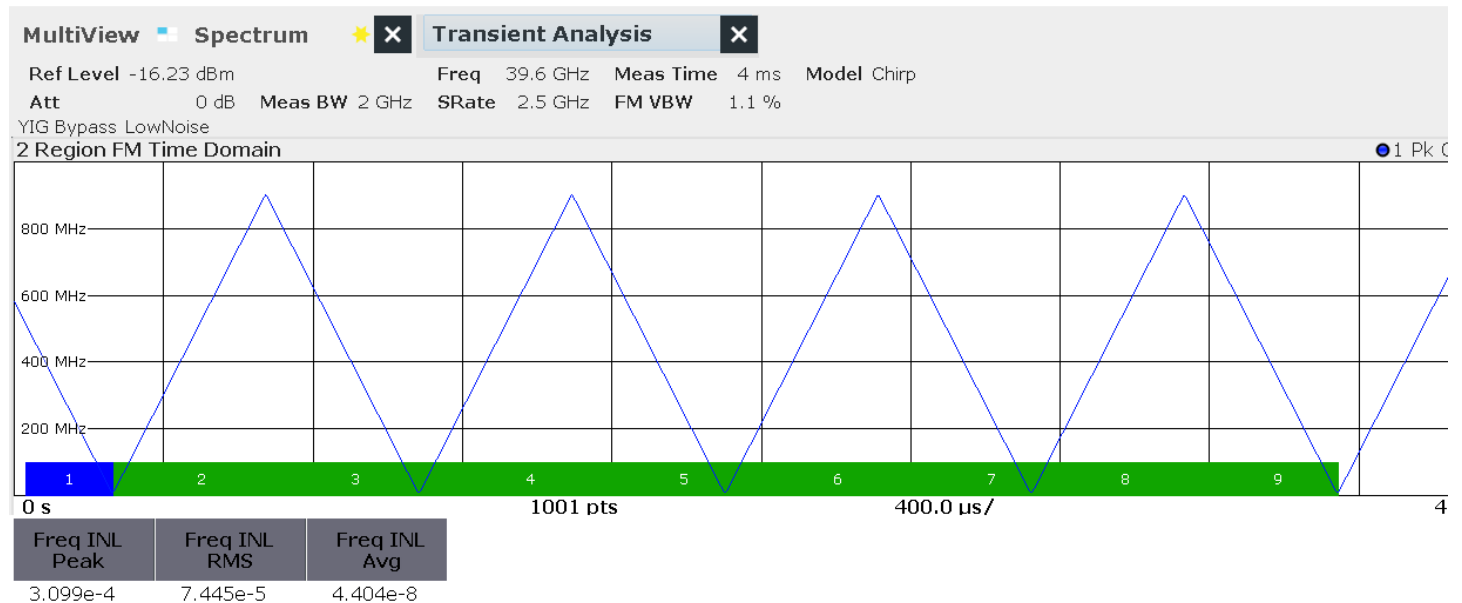
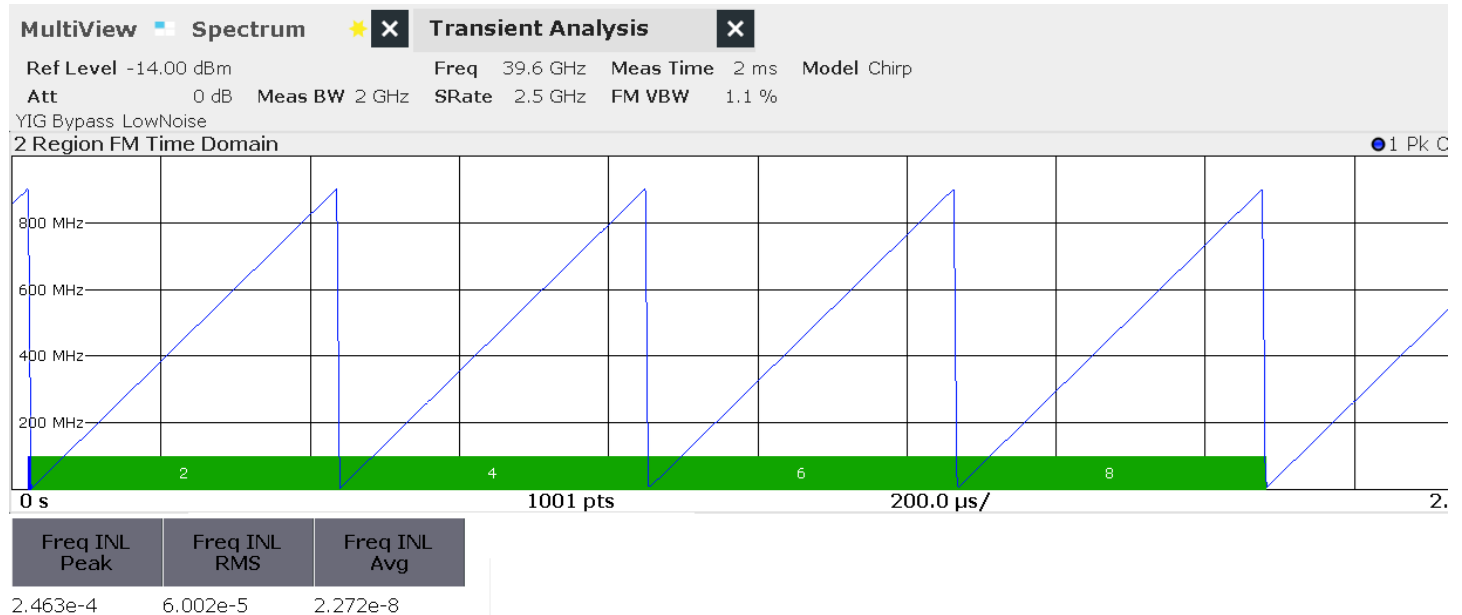
Table 7. Supported Chirp Functions – Pulse Phase Modulation

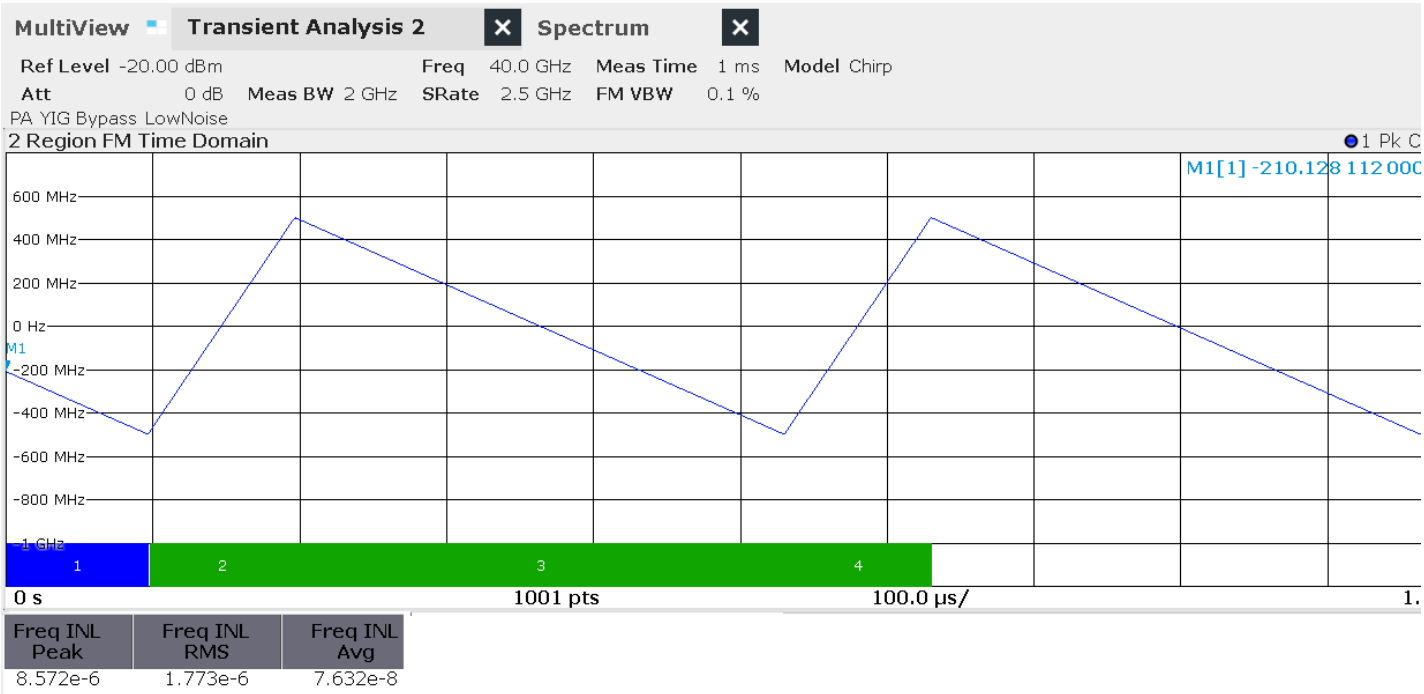
Function	Notes
Pulse Phase Modulation	
Phase Coherency Between Chirps	
True Time Delay	
Frequency-Hopped Spread Spectrum	

TYPICAL CHIRP Shapes and Linearity

Measurement parameters are: VDD = 1.8V, Ta = 25°C

The plots were captured using the Rohde & Schwarz FSW43 Signal and Spectrum Analyzer





TYPICAL PHASE NOISE PLOTS

Measurement parameters are: VDD = 1.8V, Ta = 25°C

The plots were captured using the Keysight E5052B Signal Source Analyzer and Keysight N9032B Signal Analyzer

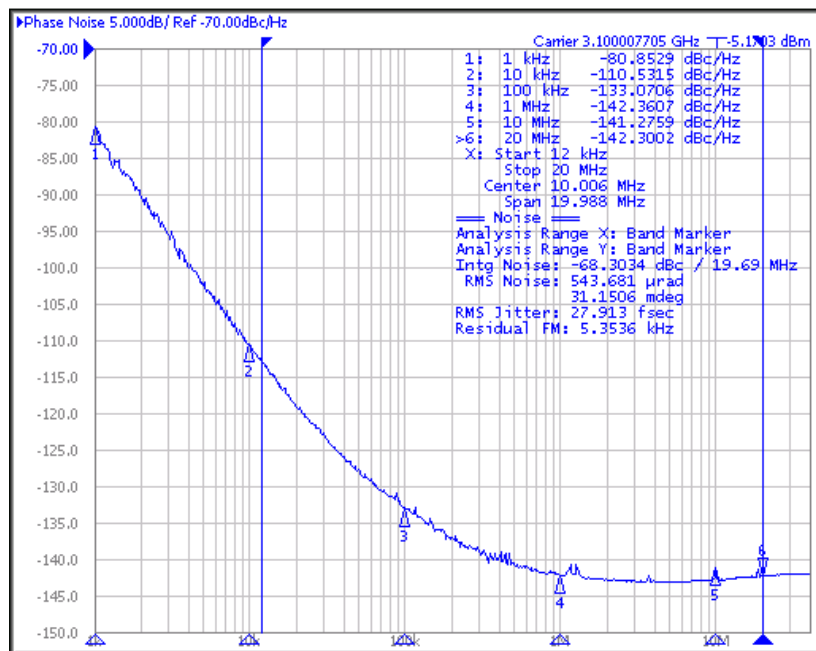


Figure 2. Fout = 3 GHz

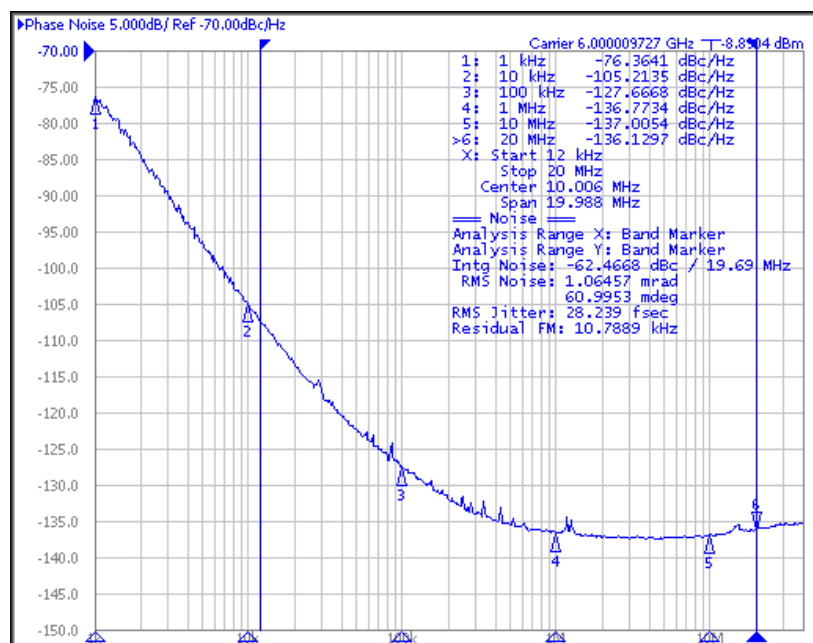


Figure 3. Fout = 6 GHz

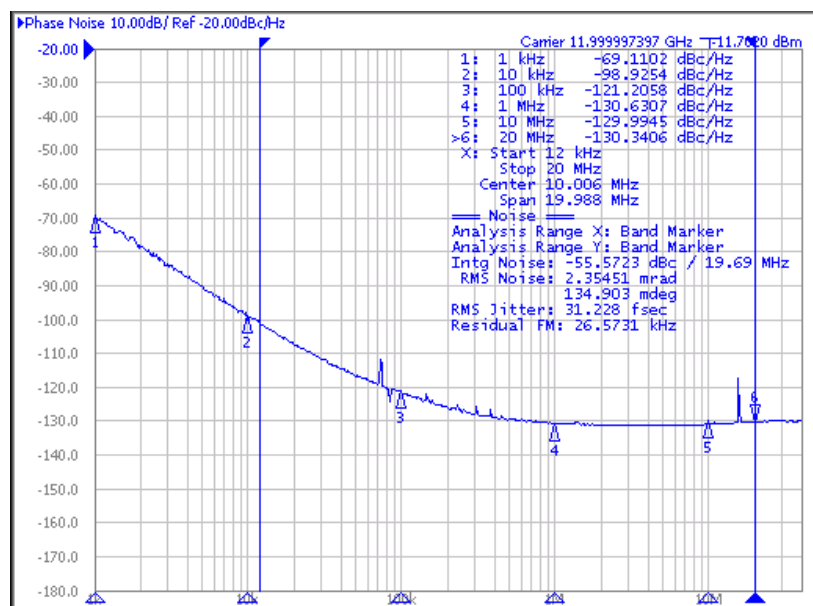


Figure 4. Fout = 12 GHz

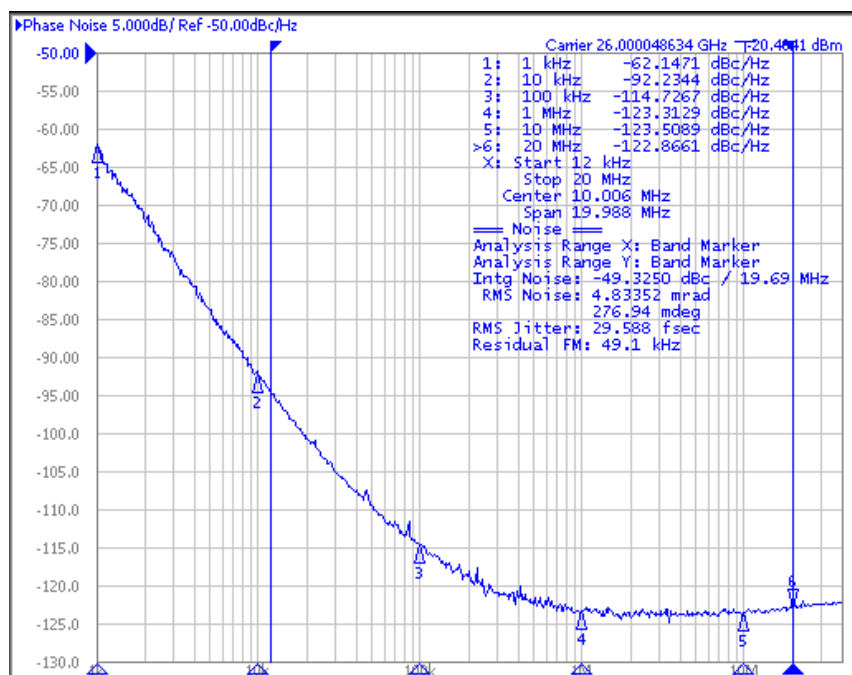


Figure 5. Fout = 26 GHz

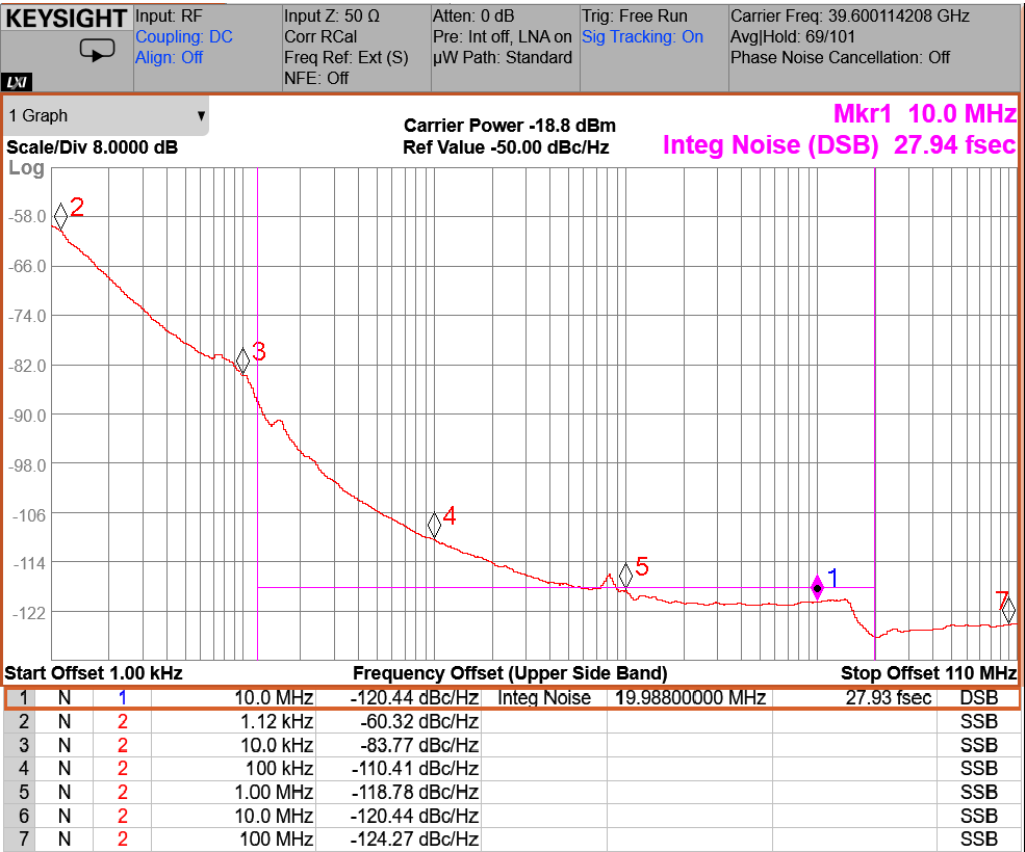
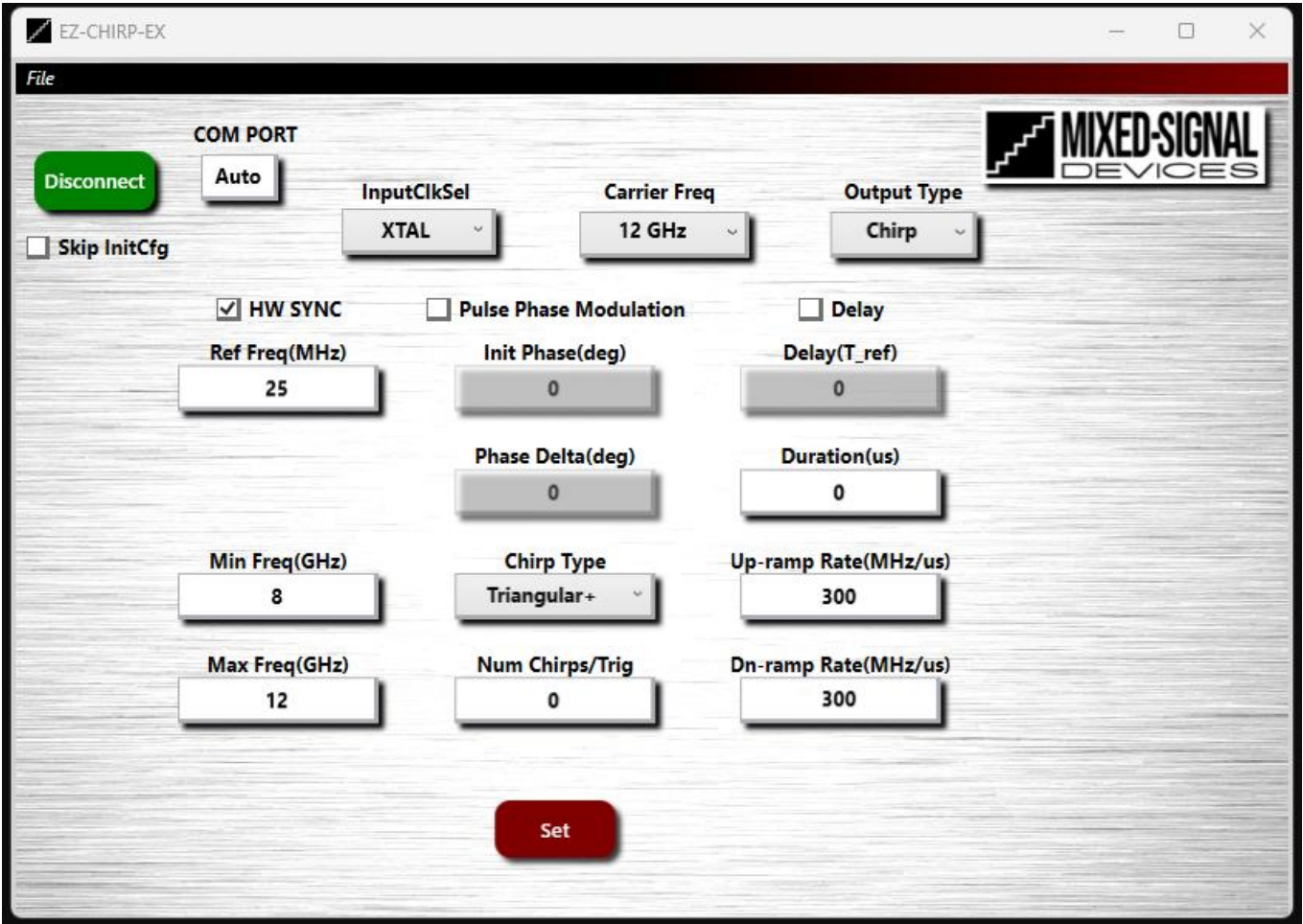


Figure 6. Fout= 40 GHz

The EZ-CHIRP-EX Applications GUI



PIN ASSIGNMENT AND DESCRIPTION

Mixed-Signal Devices Inc.
October 29, 2025

Pin 1	1	2	3	4	5	6	7	8
A	GND	RF3G_P	RF3G_N	GND	SPI_SEL	SDA	SYNC_IN	SS_CLK
B	RF6G_N	GND	GND	GND	ICLK	SCL/SCLK	SYNC_OUT	SS_SYNC
C	RF6G_P	NC	NC	VDD	GND	VDD	SSEL	SS_DATA
D	GND	NC	VDD	VDD	AUX_P	AUX_N	MOSI	GND
E	RF12G_N	GND	VDD	VDD	NC	OE	GND	NC
F	RF12G_P	GND	VDD				VDD	NC
G	GND	GND	VDD	VDD	GND		VDD	VDD
H	GND	GND	RF25G_P	RF25G_N	GND	RF40G_P	RF40G_N	GND

Figure 7. MS4000 Pin Assignments

Table 8. MS4000 Pin Descriptions

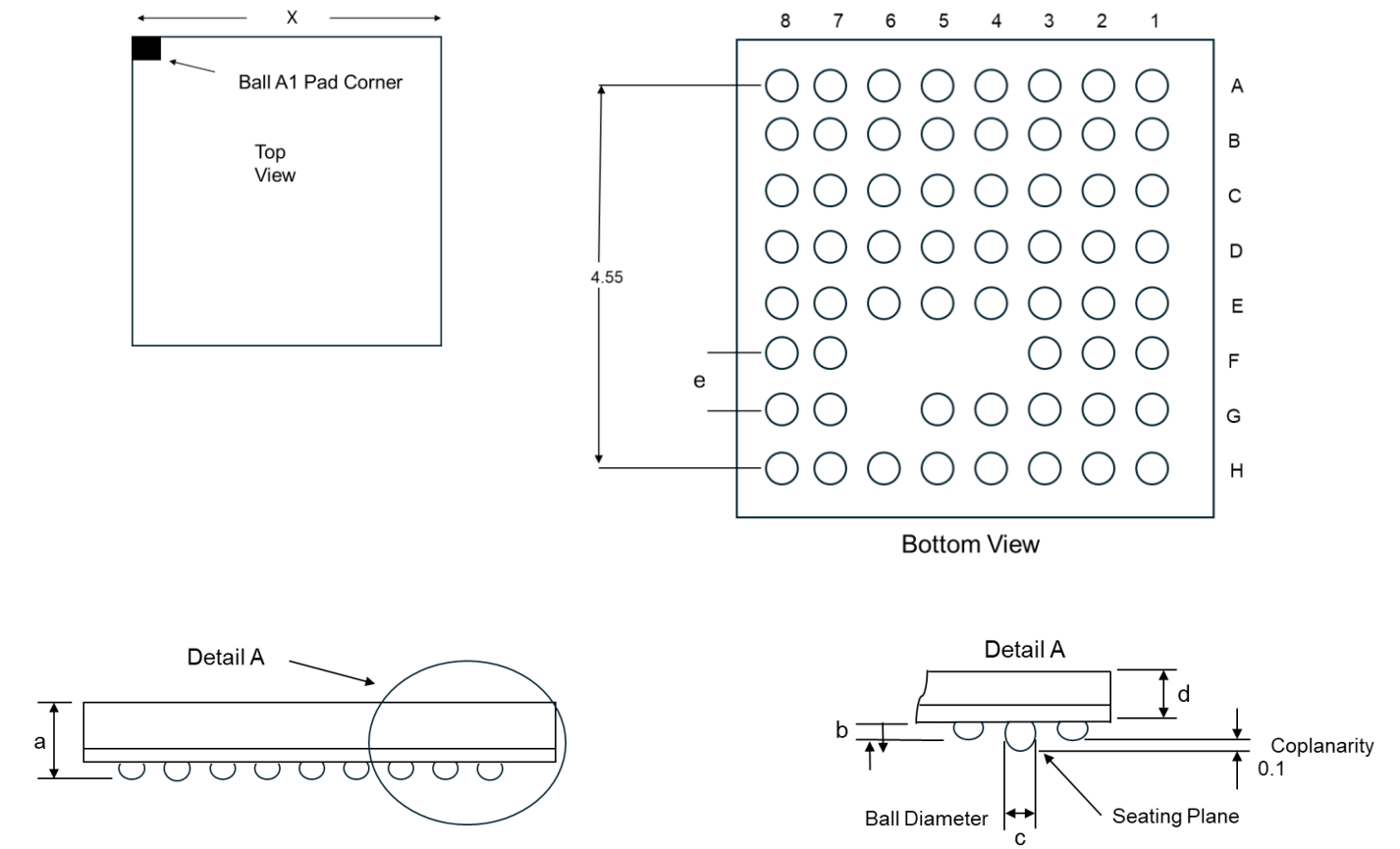
Pin No.	Name	I/O	Description
A5	SPI_SEL	I	SPI Select: SPI=1; I ² C =0
A6	SDA	I/O	I ² C Data
B6	SCL/SCLK	I	I ² C /SPI Clock
C7	SSEL	I	SPI: SSEL
D7	MOSI	O	SPI: MOSI
E6	OE	I	Output Enable
A7	SYNC_IN	I	Synchronized pulse input
A8	SS_CLK	I	Sync Clock
B7	SYNC_OUT	O	Synchronized pulse output
C8	SS_DATA	O	Synchronized Input data
D5	AUX_P	I	Differential input clock
D6	AUX_N		
B5	ICLK	I	Single-ended input clock
A2	RF3G_P	O	Differential RF Output, 2 – 3.5 GHz
A3	RF3G_N		
B1	RF6G_N	O	Differential RF Output, 4 – 7 GHz
C1	RF6G_P		
E1	RF12G_N	O	Differential Output, 8 – 14 GHz
F1	RF12G_P		

Table 8. MS4000 Pin Descriptions

Pin No.	Name	I/O	Description
H3	RF25G_P	O	Differential RF Output, 24 – 27 GHz
H4	RF25G_N		
H6	RF40G_P	O	Differential RF Output, 36 – 42 GHz
H7	RF40G_N		
C2,C3,E5,D2,E8,F8	NC		No Connect
C4,C6,D3,D4,E3,E4,F3,F7,G3, G4,G7,G8	VDD	PWR	1.8V Power Supply
A4,B2,B3,B4,C5,D1,D8,E2, E7,F2,G1,G2,G5,H1,H2,H5,H7	GND	GND	Ground

PACKAGE INFORMATION

Outline Dimensions



Dimensions	Min	Nom	Max
a	1.236	1.386	1.536
x	6 BSC		
x	6 BSC		
b	0.22	0.32	0.42
c	0.35	0.4	0.45
d	1.016	1.066	1.116
e	0.65 BSC		
Package Edge Tolerance	0.1		
Mold Flatness	0.1		
Coplanarity	0.1		

Figure 8. MS4000 Packaging Drawing

Thermal and Environmental Characteristics

Table 9. Package Thermal Conditions

Package	Parameter	Symbol	Value	Unit
6 mm x 6 mm 60 pin BGA	Thermal Resistance, Junction to Ambient	θ_{JA}	60	°C/W
	Thermal Resistance, Junction to Board	θ_{JB}	30	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T _j	125	°C
The thermal condition is based on JEDEC PCB condition (JESD51-5) and is for reference only. The actual value varies with PCB design.				

Table 10. ESD Levels

Description	Description	Specification	Level
HBM ¹	Human Body Model	JEDEC JS-001	1000V
CDM ²	Charge Device Model	JEDEC JESD22-C101	250V
Notes:			
1. 1000V HBM allows safe manufacturing with standard ESD control process – JEDEC document JEP155			
2. 250V CDM allows safe manufacturing with standard ESD control process – JEDEC document JEP157			

Table 11. Environmental Compliance

Parameter	Test Condition
Moisture Sensitivity Level (MSL)	4
Note: For additional information not listed, please contact Mixed-Signal Devices.	

DEVICE TOP MARKING

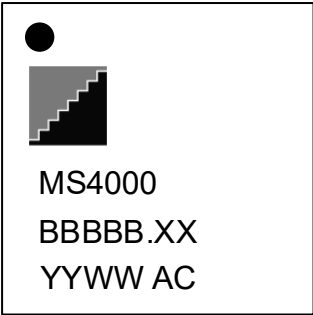


Figure 9. MS4000 Device Top Marking Showing Pin 1

Table 12. MS4000 Device Marking Legend

Line	Position	Description
1	1	Pin 1 Orientation Mark (Dot)
2	1	Mixed-Signal Logo
3	1-6	Product Marking
4	1-5	Wafer Lot Number
	6-7	Wafer #
5	Lot Trace Code	
	1-2	Year (last two-digit of the year)
	3-4	Calendar Work Week Number (1-53)
	5-6	Assembly Code

Figure 10 shows the reflow profile for MS4000

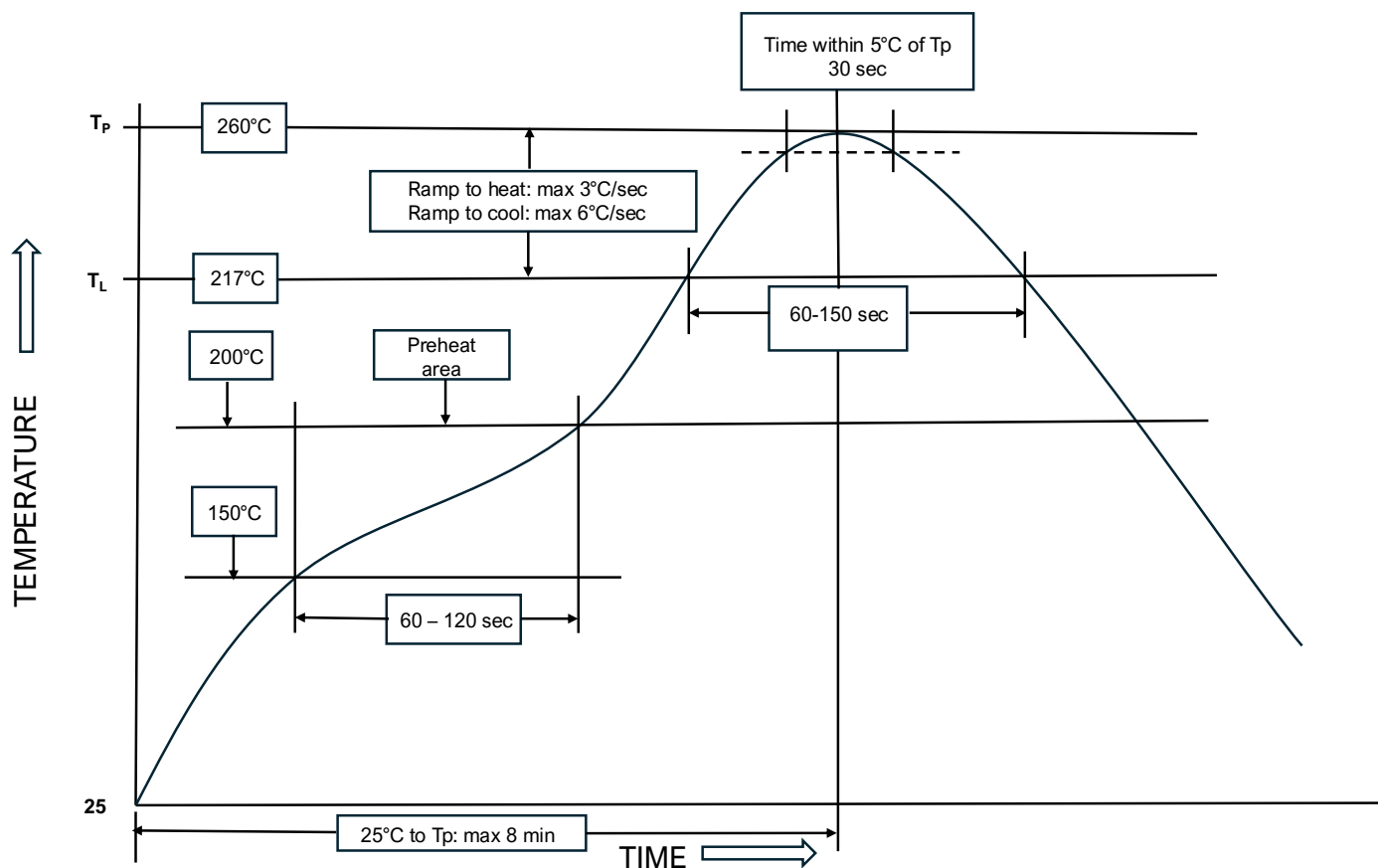


Figure 10. MS4000 Reflow Profile

REVISION HISTORY

Revision 1.1

October 29, 2025

- Updated RFOUT1 Frequency range from 3-8GHz to 3-7GHz
- Added reflow profile

Revision 1.0

September 5, 2025

- Initial Release

IMPORTANT NOTICE AND DISCLAIMER

MIXED-SIGNAL DEVICES INC. PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

Mailing Address: Mixed-Signal Devices Inc, 2 Venture, Suite 300, Irvine, California 92618, USA Copyright © 2024.